Double-Sided Cooling and Thermo-Electrical Management of Power Transients for Silicon Chips on DCB-Substrates for Converter Applications: Design, Technology and Test

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Abstract

This paper deals with the system design, technology and test of a novel concept of integrating Si and SiC power dies along with thermo-electric coolers in order to thermally manage transients occurring during operation. The concept features double-sided cooling as well as new materials and joining technologies to integrate the dies such as transient liquid phase bonding/soldering and sintering. Coupled-field simulations are used to predict thermal performance and are verified by especially designed test stands to very good agreement. This paper is the second in a series of publications on the ongoing work.

1 INTRODUCTION

Novel concepts in power electronics rely heavily on the availability and processability of new materials and packaging technologies to meet the requirements of increasing performance and reliability at lower form factor, weight and cost. This will also become apparent for the contemplated system in this paper: Twelve Si power dies (typical six-pack converter) for industrial applications needs to be cooled with a limited thermal budget and integrated into a commercial standard casing. Thermal transients need to be managed by implementation of a thermo-electric cooler (TEC) and the excess heat rejected into the environment. So the envisaged packaging and cooling concept looks as shown in Figure 1.

![Cooling Concept](Image)

**Figure 1: Schematic of the targeted packaging concept.**

This design (for a more detailed exposition see [1]), allowing a very compact architecture due to the double sided cooling and smart TEC-driven power transients management, there are several challenges concerning system design and joining technology. Among those are:

- Hi-temperature joining material hierarchy in flip-chip mounted power dies (IGBTs) on direct copper bonded (DCB) substrates,
- Hi-Voltage insulation of flip-chip mounted dies and contacting of buried gate,
- System-level TEC mounting at low bond line thickness (BLT) and high thermal conductivity thermal interface material (TIM),
- DCB-warpage tolerant design and processes,
- Unknown reliability and thermo-mechanical interactions,
- Back and front side heat removal or storage,
- Electrical contacts and EasyPIM integration.

<table>
<thead>
<tr>
<th>Table 1: Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quantity</strong></td>
</tr>
<tr>
<td>Total normal power module</td>
</tr>
<tr>
<td>Total overload power module</td>
</tr>
<tr>
<td>Normal power per IGBT</td>
</tr>
<tr>
<td>Overload power per IGBT</td>
</tr>
<tr>
<td>Total Overload Power IGBT</td>
</tr>
<tr>
<td>Overload power per Diode</td>
</tr>
<tr>
<td>Overload time</td>
</tr>
<tr>
<td>Max. Heat sink temperature</td>
</tr>
<tr>
<td>Max. junction temperature</td>
</tr>
<tr>
<td>Max. T, increase during overload</td>
</tr>
</tbody>
</table>

All this calls for an integrated approach centred on technology development using design as well as verification at all stages and for all parameters of interest. So whereas the requirements, drivers, justifications, literature search and alternatives for the given design as well as first layout simulation, feasibility studies and characterisation tools have been outlined in detail in [1], this paper will go further to address the technological realisation and thermal
management concept. In particular, the concept will attempt buffering the heat generated by the transients on the top side by a phase change material system instead of using a second cold plate.

For quick reference, here once again the specifications and ratings are given in Table 1.

2 PROOF OF THERMAL MANAGEMENT CONCEPT

To validate the double-sided cooling approach with TEC cooling and transient heat buffering before embarking on the full converter design, it was decided to furnish the proof of concept on a demonstrator of reduced complexity. This device will focus on the thermal performance, employing standard joining materials and technology. Both experiment and simulation are employed first to all individual building blocks of the concept before their agreement is shown on system level.

2.1 Concept RC-Demo

This Reduced Complexity Demo (RC-Demo) shows only a one-dimensional heat path from one Mosfet via a TEC to a heat-sink on every side (see also [1] for details). This is schematically depicted again in Figure 2.

![Figure 2: Schematic RC-Demo.](image)

As can be seen, the MOSFET is assembled on AlN substrate and fixed on a heat sink. On the top side of the MOSFET a TEC is assembled to realise the top side cooling. As the knowledge of the temperature gradient of the TEC is necessary for the investigation the TEC enhanced cooling, the temperatures of both sides of the TEC are measured. For the bottom side temperature a 110 µm Silicon diode is integrated. The top side temperature of the TEC is measured by a metal based heat flow sensor, which allows the heat flow and contact surface temperature measurement. With external controller one can adjust transient power losses in MOSFET and also transient control of TEC current and thus TEC heat pumping.

To focus the setup as much as possible to the effect of TEC-enhanced cooling, the device selected for the RC-Demo is a 25V MOSFET packaged into a metallic package (CanPAK™), which enables double-sided cooling, when mounted appropriately [3].

The heat path from the power module goes (Figure 2):

- Down directly to the AlN substrate.
- Up, through a diode (serving as temperature sensor) and a TEC to a copper socket (serving as heat flux sensor).

2.2 Technology RC-Demo

The joints on every interface have been optimized in terms of voiding to assure a minimal thermal resistance on those heat paths.

The assembly process flow was particularly challenging, because of the different size and nature of the stacked components and their interface materials. We developed two different assemblies, one with and the second without TEC, to compare the effect of adding a TEC inside such a stack to perform double sided cooling.

First, the CanPAK and some passive components have been soldered to the AlIN substrate. This solder process has been optimized to perform joints with a low amount of voids.

Our aim was to reduce the voiding to less than 10% inside the complete joint. The classical process soldering process on such large areas gave a voiding of about 30% as shown in Figure 3 (left). By using a special solder paste for low void applications, a reflow oven capable of heating under pressure-vacuum cycles and an optimisation of the reflow profile and the way of dispensing the solder paste, we were able to reduce the voiding repeatedly to under 7% as shown in Figure 3 (right).

![Figure 3: X-ray analysis of soldering process optimisation. With default process parameters (left) with optimized process parameters (right).](image)

For the version with TEC, the TEC was soldered with the same low voiding process to the diode. Afterwards, the lower side of the diode was glued to the upper side of the CanPAK using thermally conductive glue and spending attention to the planarity and width of this gluing joint to limit the thermal resistance of this interface.

Once the stack assembled, the contacts from diode and TEC to the substrate have been formed by Au wirebonds of 25 µm. On each pad, umpteen bonds have been performed to increase the maximum admissible current. The wire bonds have been realised on an area overlapping the underneath component as shown in Figure 4. These bonds have been encapsulated for protective reasons.

![Figure 4: Wire bonds to connect chip diode and TEC module to AlN substrate.](image)
The Cu socket (thermal current sensor) was added on the measurement base, and its interface to the TEC was liquid metal for lowest thermal resistance. The final assembly is shown in Figure 5.

2.3 Thermo-electrical modeling

The modelling of thermo-electric coolers and generators can easily be done by applying appropriate TEC-current dependent heat flow and heat generation loads within a thermal simulation. But since the pumping power is a function of the absolute temperature (DOF to solve) a coupled electro-thermal simulation is much more accurate, especially within transient simulations where a range of temperatures occurs, hence you cannot iteratively adjust the Peltier coefficient to improve the result.

\[ e = \alpha T \]  

(1)

In [1] an effective electro-thermal finite element model of TEC coolers has been introduced, which reduces the TEC-couples to one active layer with effective material data, emulating the thermo-electric behaviour of the complete structure: thermo-couples, metallization layers and thermal interfaces. The models are very easy to implement, not needing a high amount of elements, which helps especially in large simulations at system or device level.

The thermal conductivity \( \lambda \), electric conductivity \( \kappa \) and Seebeck coefficient \( \alpha \) of the active layer are determined by an optimizing (error minimizing) simulation loop (Figure 6) of datasheet values and also RC-demo experiments, varying the TEC current \( I_{TEC} \), the TEC’s heat load \( P_{TEC} \) and the TE layer temperature \( T_{TEC} \).

For the micropelt TEC mpc-d701 the material parameters are given in Table 2, also considering temperature dependent data that has been added manually to fit the performance data more accurate (\( \varepsilon_T = 0.1 \) K). In addition a 15% degradation of the figure of merit \( Z \) at high temperatures (beyond measured data) has been considered. An optimization algorithm that inputs polynomial fits for \( \lambda(T), \kappa(T) \) and \( \alpha(T) \) is still under development.

Table 2: temperature dependent material data for transient modelling of the microPelt TEC mpc-d701 active layer [4]

<table>
<thead>
<tr>
<th>Temperature [°C]</th>
<th>3</th>
<th>25</th>
<th>33</th>
<th>60</th>
<th>80</th>
<th>120</th>
</tr>
</thead>
<tbody>
<tr>
<td>Th. conductivity [W/mK]</td>
<td>0.394</td>
<td>0.398</td>
<td>0.402</td>
<td>0.411</td>
<td>0.422</td>
<td>0.439</td>
</tr>
<tr>
<td>El. Resistivity [µΩm]</td>
<td>216</td>
<td>216</td>
<td>216</td>
<td>216</td>
<td>216</td>
<td>225</td>
</tr>
<tr>
<td>Seebeck coef. [µV/K]</td>
<td>285.4</td>
<td>287.3</td>
<td>288.1</td>
<td>290.6</td>
<td>293.8</td>
<td>282.1</td>
</tr>
</tbody>
</table>

For the silicon substrates temperature dependent density \( \rho \) and specific heat \( c_p \) was defined by literature data. As can be seen for the active layer no density and specific heat was defined. The relatively thin structure has a minor impact on the transient behaviour of the TEC.

In general, transient data evaluation (\( \rho \) and \( c_p \)) can be done separately after static (\( \lambda, \kappa \) and \( \alpha \)) data evaluation which is important to know to reduce the number of adjustment or optimization parameters and calculation time. Also the transient behaviour is not influenced by interface effects or defects. So literature data of well-known materials (Si in case for the mpc-d701) will already be in good agreement, making optimization loops less necessary.

2.4 Thermal Characterisation

To demonstrate the effect of the double side cooling using TEC the RC-demo was used to simulate different load scenarios. The MOSFET can be controlled to generate a certain heat and the TEC module can be driven by specified electrical current. The temperature as well as the heat flux in both directions can be measured in-situ. The Figure 7 shows one of the experiments to investigate the TEC effect. The experiment contains three load steps.

In the first step the TEC and the MOSFET were switched off (to measure the current thermal steady state of the setup), where the diode temperature measured 70.6 °C.

In the second load step the MOSFET was operated to generate \( P = 3 \) W of thermal load during the TEC kept switched off. The diode temperature was 76.3 °C after reaching steady state.

To simulate the over load situation of the MOSFET the power of the MOSFET was increased step wise in the third step to four watts and in the same time the TEC was switched on using \( I = 0.4 \) A electrical current (to study the influence of the transient cooling effect).

As it can be seen in Figure 7 the diode temperature decreased to 72.5 °C (-3.8 K).
Figure 7: Selected transient result of RC-demo experiment.

Figure 3d shows the results of the heat flow for all three scenarios at different operation temperatures. The red bars show the back side heat flow (to substrate) the blue one shows the heat flow pumped by the TEC. It can be seen, that the heat flow to the top site increase from 0.39 W to 2.5 W due to the pumping effect of the TEC (for 70°C operation temperature).

Figure 8: Pumped heat by TEC module (blue) and heat fluxes via substrate and backside cooling (red) for different mean temperatures (30 °C, 50 °C and 70 °C).

By the design of the RC-demo it is only possible to measure temperatures at certain locations (see Figure 2). For a better understanding and evaluation of the heat path concept more information regarding the temperatures and heat fluxes would be desirable. For this purpose non-contact, infrared imaging was used to extract more important information.

One side of the RC demos was for reasons of measurement accuracy covered with a black paint.

Figure 9: IR image of RC-demo activated TEC.

Figure 9 shows the selected field of view for the investigations. Beginning from bottom the MOSFET, chip diode, TEC module and Cu-socket (partly) can be seen by the infra-red camera.

In addition to the transient measurements to verify the simulation models and results of experiments (See Figure 7) a study on the pumped heat and temperature gradients of the active TEC layer was carried out. At constant thermal boundary conditions, the temperature fields were measured (on the prepared side) and evaluated for different TEC currents. (See Figure 9)

Figure 10: IR image for different TEC currents and path for evaluation.

As expected and can be seen in the infra-red images (Figure 10) with increasing TEC current the average temperature and the temperature of upper TEC layer increases.

The evaluation of the temperatures along a path (starting in the upper central edge of the image to the bottom) the associated temperature gradient across the active TEC layer and heat flow upwards are summarized in Figure 11.
Temperature gradients increase from 5 K to 25 K. Also the pumped heat increases from 0.26 W up to about 2 W (increasing slope of line). These results fit very well to the transient results of RC-demo.

By means of transient experiments and the infra-red imaging the effectiveness of the selected cooling concept could be proven. It has been shown that the junction temperature (chip of the diode) can be kept constant or reduced even under additional overload losses.

3 POWER MODULE DESIGN

DCB layouting was done in consideration of the final casing capping the power module. The choice was oriented on the EasyPIM casing, delimiting as such the final DCB outline. The casing allows with the use of pins the contact feeding from the cased DCB substrate towards the top of the polymer casing where a PCB can be mounted and connected to the pins. The Figure 12 depicts an exploded view of the targeted module.

The layout of the bottom DCB enables the assembly of 6 IGBTs and 7 diodes (6 for the converter, the last one acting as a thermal sensing diode). The layout of the upper DCB, mounted over the power devices for the double sided concept, encloses spaces on its upper layer for mounting 6 TECs over each aggregate “IGBT+Diode” and wirebonding areas for power supply of the TECs as depicted in Figure 13. From the top of the TECs the heat can is to flow to a top-mounted heatsink or thermal buffer.

**Figure 12: exploded CAD view of the targeted module.**

## 3.1 Thermal Simulation

The considered new technology also includes new materials that are not yet been characterized w.r.t. thermal conductivity. For this reason, effective material data from the compositions of TLPB and TLPS were generated by using volume proportions of the components. A cross section (Figure 22) was used to count the proportion of copper and Cu₆Sn₅. About 25% pure copper was determined in the present sample. The results are presented in Table 3.

### Table 3: Effective thermal material data for TLPS layer

<table>
<thead>
<tr>
<th></th>
<th>Cu₆Sn₅</th>
<th>Cu</th>
<th>effective</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proportion [%]</td>
<td>75</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>Conductivity [W/m K]</td>
<td>34,1</td>
<td>386</td>
<td>122,1</td>
</tr>
<tr>
<td>Specific heat [J/kg K]</td>
<td>286</td>
<td>384,7</td>
<td>310,7</td>
</tr>
<tr>
<td>Density [kg/m³]</td>
<td>8280</td>
<td>8827</td>
<td>8416,8</td>
</tr>
</tbody>
</table>

A TLPB layer typically consists of an intermetallic phase Cu₆Sn₅ in the core surrounded by two thinner layers with Cu₃Sn. Weighted by the proportionate thicknesses effective material data is also generated for TLBP as shown in Table 2.

### Table 4: Effective thermal material data for TLPB layer

<table>
<thead>
<tr>
<th></th>
<th>Cu₆Sn₅</th>
<th>Cu₃Sn₅</th>
<th>Cu₃Sn</th>
<th>effective</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness [µm]</td>
<td>2</td>
<td>6</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Conductivity [W/m K]</td>
<td>70,4</td>
<td>34,1</td>
<td>70,4</td>
<td>43</td>
</tr>
<tr>
<td>Specific heat [J/kg K]</td>
<td>326</td>
<td>286</td>
<td>326</td>
<td>302</td>
</tr>
<tr>
<td>Density [kg/m³]</td>
<td>8900</td>
<td>8280</td>
<td>8900</td>
<td>8528</td>
</tr>
</tbody>
</table>

However, it is very important to note that these are only assumptions. As already shown by the authors in [2] there is a strong dependence on the process parameters on the thermal material properties of a mono-metal interconnect (sintered silver die attach). Therefore, the material characterization taking into account the processes conditions as in [2] is a necessary next step to ensure the quality of the simulation results.

The thermal simulation model includes six IGBTs and six diodes as heat-generating sources, a heat transfer coefficient on the backside of the bottom DCB and six heat flux exit areas that represent the six TECs. Three different operating modes of the converter module are simulated. Normal operation, an overload scenario with no increase of max junction temperature of IGBT and an overload scenario with +5 K permitted junction temperature rise.

The thermal boundary conditions (derived from Table 3) are summarized in Table 5 and Figure 14.
Solving the model led to a slightly asymmetrical temperature distribution in bottom DCB (Figure 15, left). IGBTs near to the border are about 5 K hotter. The reason for this is the slightly asymmetrical design of the entire module (see Figure 14Figure 3 bottom).

By varying the heat pumped by the TECs both overload situations can be depicted with this model. To have same maximal junction temperature in overload the six TECs need to pump 3.7 W each. (See figure 4 left and right). 3.3 W per TECs are necessary if +5K in maximal junction temperature is permitted.

As result of these investigations it can be stated that transient double sided cooling supported by thermo-electrical cooler are suited to overcome transient overload situations in a power package. A further important question is how the overload heat and the additional energy needed for pumping can be stored (Buffering of Thermal Transients) will discussed further below.

### 3.2 Buffering of Thermal Transients

The simulations of TE cooler assisted heat buffering devices with phase change materials have shown that multiple design aspects are critical and have to be addressed carefully. Figure 16 shows the buffering system and an equivalent circuit for a one-dimensional design estimation concerning the TE coolers and the buffer (PCM component). While the other thermal resistances can be considered as thermally transparent to the system, the phase change buffer has to be handled as a thermal transmission line (by analogy to electrical system design) because of its high specific heat during phase change and thus low diffusivity. However, the problem of temperature diffusion will be ignored at first, to get a starting point for the TEC and buffer design.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Overload Normal</th>
<th>Overload +0K</th>
<th>Overload +5K</th>
</tr>
</thead>
<tbody>
<tr>
<td>P_IGBT [W]</td>
<td>11.6</td>
<td>17.6</td>
<td>17.6</td>
</tr>
<tr>
<td>P_diode [W]</td>
<td>1.6</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>Q_TEC [W]</td>
<td>0</td>
<td>6x3.7</td>
<td>6x3.3</td>
</tr>
<tr>
<td>Heat transfer (backside) [W/m²K]</td>
<td>1380</td>
<td>1380</td>
<td>1380</td>
</tr>
<tr>
<td></td>
<td>70 °C</td>
<td>70 °C</td>
<td>70 °C</td>
</tr>
</tbody>
</table>

**Figure 14:** Overview of model and thermal boundary conditions.

**Figure 15:** Temperature fields normal operation (left) and overload operation with activated transient cooling (TECs=on).

**Figure 16** Thermal equivalent circuit of a transient TEC-assisted buffering system using a phase change material.

### Table 5: Overview of thermal boundary conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>a, b, l</td>
<td>Dimensions of the effective TE layer</td>
</tr>
<tr>
<td>α, λ, σ</td>
<td>seebeck coeff., thermal conductivity and el. resistivity of the effective TE layer</td>
</tr>
<tr>
<td>T_C, T_hot, ΔT_TEC, P_{ hot, TEC}</td>
<td>cold and hot side temperature, temperature difference and power loss of the TEC</td>
</tr>
<tr>
<td>T_{ hot, P_{ hot}}</td>
<td>Hot spot temperature and overload, power that has to be stored</td>
</tr>
<tr>
<td>R_1</td>
<td>thermal resistance of the layer structure between hot spot and TEC (including the bordering substrate layer of the TEC)</td>
</tr>
<tr>
<td>R_2</td>
<td>thermal resistance of the layer structure between TEC and buffer (including the bordering substrate layer of the TEC)</td>
</tr>
<tr>
<td>R_{PCM}, C_{PCM}</td>
<td>thermal resistance and capacitance per unit length of the PCM buffer</td>
</tr>
<tr>
<td>L, R_s, T_{PCM}</td>
<td>length, heat sink resistance and temperature (melting temp.) of the PCM buffer</td>
</tr>
</tbody>
</table>

* values referred to one TE cooler

\[
R_s = R_{s, TOTAL} \cdot \frac{N_{TEC}}{N_{TEC}}
\]

\[
C_s = C_{s, TOTAL} \cdot \frac{N_{TEC}}{N_{TEC}}
\]

\[
P_s = P_{s, TOTAL} \cdot \frac{N_{TEC}}{N_{TEC}}
\]
**TE cooler design**

Concerning the TE cooler design, you want to make sure, that the TECs can establish the temperature control to cool the hot spot, while carrying the heat overload, which has to be buffered. The heating side of the TEC should thereby overcome the melting point of the considered PCM to initiate the phase change. Derived from one-dimensional thermo-electric theory [5-7] and using the effective TE models mentioned in section 2.3 and [1], the needed TEC’s current during the overload situation can be calculated numerically, finding the first zero of equation (2).

\[
I^2 + AI^2 + BI + C = 0 \\
A = -2abR_a(\sigma \lambda + \alpha^2(T_{in} - R_1 P_{in}) - (R_1 P_{in})R_c) \ \\
B = 2abR_a(R_1 - R_1 + T_{in}) \\
C = \frac{2a^2b^2 \lambda(T_{in} - T_{PCM} - P_{in}R_1 + R_1)}{aR_c \lambda^2} - \frac{2abP_{in}}{aR_c \lambda} \\
\]

(2)

The estimation is referred to one TE cooler used in the system. So using multiple TECs to reduce the performance requirements per TEC, the Power loss, thermal conductances and capacitances are split among the number of TECs.

It turned out, that an optimum of the number of TECs can be found concerning the system’s coefficient of performance and thus total power loss \( P_{DLot} = N_{TEC} \cdot P_{PCM} \), that has to be buffered by the buffer. As shown in Figure 17, for the envisaged thermal buffer design, a number of 15 to 20 mpc-d701 TECs would be optimal.

![Figure 17 System COP and Power loss as a function of the number of mpc-d701 TECs used.](image)

**Buffer design**

For the buffer design, a certain mass or volume of the PCM has to be provided to store the heat energy during the overload duration. A simple approximation can be given as follows, using a foam-type buffer material mix of the PCM and a thermally conductive filling material, that enhances the diffusivity of the buffer.

\[
\dot{V}_{buffer} = \frac{1}{2} \cdot \frac{P_{DLot}}{H} \\
H = M_{c} \rho_{PCM} + \Delta T_{OL} (\rho_{PCM} \cdot c_{PCM} + (1 - \zeta) \rho_{PCM}) = M_{c} \rho_{PCM} \\
\]

Table 7: Symbols used for buffer calculations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Significance</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{buffer})</td>
<td>Buffer-volume, latent heat, specific heat, density and volumetric filling factor of the PCM</td>
</tr>
<tr>
<td>(\rho_{PCM})</td>
<td>Specific heat and density of the thermally conductive filling material</td>
</tr>
<tr>
<td>(\Delta T_{OL})</td>
<td>Temperature difference between normal and overload operation</td>
</tr>
<tr>
<td>(I_{OL})</td>
<td>Overload duration</td>
</tr>
</tbody>
</table>

A thinkable PCM material mix of 65% eutectic 58Bi-42Sn [8] and 35% aluminium for example would require a volume of around 23.5cm³ for an overload scenario of 92W over 60 seconds, which would be the case for the considered power device cooling system, using 12 mpc-d701 TECs (see Figure 17). This has also been simulated within an FE analysis to investigate further design aspects on field level.

**Field Simulations**

As shown in Figure 18, four overload cycles with TEC assisted cooling have been simulated, starting with an initial non-TEC overload.

![Figure 18: 1/4 FE model of a thermal buffer system for the IGBT power device.](image)

The resulting junction temperature of the IGBT is shown in Figure 19. As can be seen, a satisfying cooling of the Power dies could not have been shown, due to different reasons.
First: The most critical issue, that has already been mentioned, is the temperature diffusion process through the buffer, during overload operation. The PCM’s diffusivity during the phase change is much too low, so that a homogeneous melting process and adequate heat buffering is cannot be guaranteed, with the current design. Figure 20 shows the inhomogeneous temperature distribution during the first TEC-assisted overload phase.

Second: Another aspect, that has to be handled, is the fact, that the stored heat within the buffer tends to “swap” back to the power dies and thus heats during the relaxation phase, because the TE coolers are turned off during this phase. So a de-ramped or post cooling phase has to be considered for the TE coolers to maintain the temperature difference between power dies and buffer. The needed TEC’s current for this phase can be estimated using equation 2 and putting the overload power $P_{OL}$ to zero. Since the post cooling current is nearly independent from the number of TECs, the TEC’s power dissipation increases with the number of TECs, which makes a high amount of TECs less attractive for the thermal buffer design.

Third: The third problem is the removal of the stored heat during the overload phase. Thus, the thermal heat sink resistance $R_h$ of the buffer and the duty cycle of overload and relaxation phase has to be set up properly. Figure 19 and Figure 21 show an insufficient heat removal during relaxation phase.

3.3 Double-Sided Cooling Technology

Building the converter with the identified IGBT and Diodes which are required for the final functional module (devices with a voltage class of 1200V) necessitates wafer level post processing prior the assembly phase itself. For this the active wafers were post processed such to achieve on one contact side of the diodes and IGBT end metallisation compatible with the assembly concept and sequence. For such the thin active device wafers were first mounted on temporary carrier wafer to enable handling during post-processing, amongst others copper and tin plating of the pads. This finishing will enable the direct use of the diced devices for assembly on standardized DCB substrates using Transient Liquid Phase Bonding (TLPB).

This bonding technology allows achieving thin bondlines resisting to high temperatures since the resulting interface consists only in intermetallic phases with decomposition temperatures far above the targeted application temperatures. The bonding process is based on tin melting and interdiffusion of copper and tin under temperature which results in a pure intermetallic bondline, only some micrometers thick.

Achieving TLPB interconnection of the active devices implies first flip-chip of the parts on their frontside to the DCB substrate. After placement, this is then directly followed by joining the devices to the substrate by heating. The thinness of the final bondline combined to its metallurgical nature, i.e the intrinsic properties of the intermetallics, should permit in a same time good electrical contact, good heat transfer to the bottom substrate and high temperature resisting interconnects, since the consisting intermetallics Cu6Sn5 and Cu3Sn have melting temperature over 400°C.

Accomplishment of the double sided cooling concept involves the mounting of a second DCB, over the backside of the power chips. This top substrate is not only required for the cooling but also fulfils electrical wiring function. Therefore up to bottom electrical connection must be conduct to close the electrical path by bringing back the wiring from the top DCB to the bottom DCB. As a consequence, top-bottom joiners are added and TLP bonded to the bottom substrate prior mounting the top DCB. Before mounting the top DCB, underfilling should overcome later possible risks of flashovers of the devices bonded to the bottom side.

The assembly of the top DCB will use Transient Liquid Phase Soldering. The principle is similar to TLPB (i.e. Obtaining a pure intermetallic bond resistant to high temperature) however with a far thicker bondline than with TLPB. Certainly this thicker bondline will imply a reduced performance in terms of a longer thermal path compared to TLPB. However, the high advantage resides here in the technological potential of final warpage compensation. A cross-section of such a joining approach is depicted in Figure 22.
Sintering can also be of advantage to manage warpage. The silver pastes are made of small silver particles evolving in a more bulky structure trough sintering. Bonds with low porosity are achieved after the process with high heat transfer ability. Even the portion of final porosity might be controlled by the process. This joining technology is also taken into account for assembling the module, sintering the power devices to the bottom side (that involves wire bonding) and for joining the top DCB.

![Figure 22 Example of a TLPS interconnect](image)

Nevertheless, as previously mentioned, the module design was established to deal with a top DCB as small as possible in respect to manufacturing design rules. This dimensioning care was implemented in order to restrain the final warpage to a still suitable proportion for assembling.

The combination of these different assembly technologies present the advantage of employing a rather low temperature assembly sequence with in the end a potential for high temperature applications and some of them might leverage risk of warpage.

### 3.4 Reliability Testing & Results

First results concerning reliability show good reliability of the sinter technology in passive thermocycling. The TLPS joining technology seems more critical in passive thermocycling. However for this testing method, the DCB substrates are the most sensitive parts, that will lead to a faster failing of the module. The use of dimples can increase the lifetime of sustrate however at the expense of compactness/packing density of the module.

### 4 CONCLUSIONS & OUTLOOK

In this paper we showed a comprehensive approach to a novel power converter design including simulation, technology and test. New joining technologies could be shown to enable this novel thermal management concept featuring double sided cooling along with thermal buffering as the only viable heat rejection mechanism via TEC devices. Simulations have shown the thermal feasibility, successful display of joining technologies allows now a sequential die attach on both sides without remelting. Thus, the fundamental requirements of the new architecture are met. Next steps will consist in module assembly and system characterisation as well as reliability considerations. This will be published in another paper soon.

**Acknowledgements**

The authors gratefully acknowledge their funding by the EU FP 7 Integrated Project “Smartpower”, Grant #288801.

**Literature**


