# Transient Thermal Management by Using Double-Sided Assembling, Thermo-Electric Cooling and Phase-Change Based Thermal Buffer Structures: Design, Technology and Application

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*Abstract*

*In this paper, a cooling concept for power electronics is discussed, using thermo-electric cooling in combination with a phase-change based latent heat storage module. It was designed to cope with thermal transients due to periodic overload operation phases of an IGBT power converter module. Several sub-system simulations and experiments have already been performed in previous publications leading to the current design state, which is now being tested under emulated experimental conditions. Very good results are presented, showing the feasibility of the transient cooling concept. On-going work referred to the long-term thermal stability and operation as well as a smart electrical TEC control will be motivated.*

## 1 Introduction

Dealing with the increasing performance and reliability requirements of today's power electronic, new materials and integration concepts are one of the main focuses of the on-going packaging research. In this context, the thermal system design is mainly determined by covering higher power densities because of the trend of reduced form factors and increased power losses within the integrated systems and modules. Thus, managing hot spots as well as cooling the system within a limited footprint are the problems to deal with.

Along with the development of new materials and assembling technologies leading to decreased thermal resistances from junction to case, more sophisticated attempts are investigated, which implement thermo-electric layers and cooler modules into the thermal paths of the devices. These would act as a temperature control unit that could actively cool hot spots and mitigate critical temperature distributions [15 - 20].

An improvement of the system cooling however is difficult because of the additional power loss, these modules come with. To effectively cool a thermal system, the TEC's net cooling performance $\Delta T_{TEC}$ has to exceed the amount of additional temperature drop that is caused by the TEC's power loss $P_{TEC}$.

Otherwise, there is no cooling effect at all (eq. 1).

$$\Delta T_{TEC} \overset{!}{>} R_{th,TEC-amb} P_{TEC} \qquad (1)$$

Besides an already mentioned reduction of the thermal resistances, one of the key parameters is the efficiency of the TEC, namely the TEC's figure of merit $ZT = \alpha^2 T/\lambda/\rho$. It mainly determines the net cooling performance ($ZT\uparrow$ $\Delta T_{TEC}\uparrow$) as well as the coefficient of performance, thus the TEC's power loss ($ZT\uparrow$ $P_{TEC}\downarrow$). Therefore a lot of material research activities try to maximise the seebeck coefficient and electrical conductivity while maintaining a low thermal conductivity. This would enable a sufficient thermo-electric performance in order to make TE structures a feasible thermal design tool for cooling down lossy power devices.

Another attempt which is pursued in this work is the circumvention of the thermal resistance $R_{th,TEC\text{-}amb}$, by keeping the heat within the thermal system. In this way, the (mostly dominant) high temperature drop at the (in most cases) convective final thermal resistance to ambient is avoided by using a thermal storage module or phase change based latent heat buffer. This solution is designed to cope with thermal transients occurring in today's electronics and to provide a temporary infinite thermal capacitance in conjunction with a TE cooling module.

As already explicitly discussed in [1, 2 and 3], the cooling strategy will be demonstrated within an IGBT power converter module, that is envisaged to be capable of temporary overload operations (see figure 1).

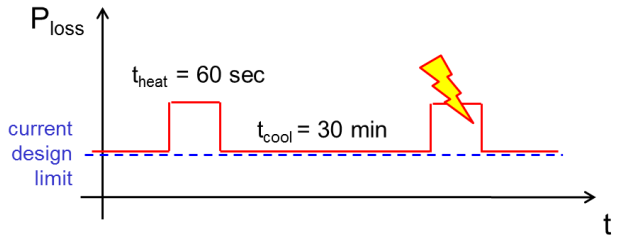


*Figure 1: Envisaged loading conditions for the improved thermal system design*

A double-sided cooling approach is applied using a top-sided TE cooler and a heat pipe enhanced and phase change based latent heat storage device for temporary heat storage. This novel concept will be implemented into an industrial PIM package standard with the thermal buffer module protruding from (figure 2). A geometrical insertion of the cooling module will have to be done in a later concept optimisation phase.

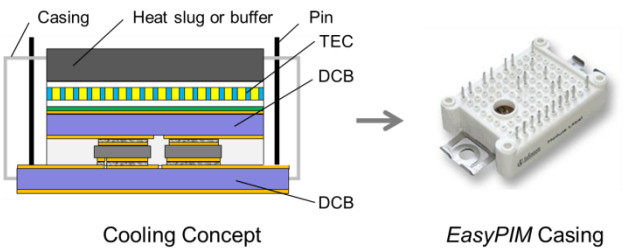


*Figure 2: Schematic of the targeted packaging concept*

## 2 Enabling Joining Technology and assembling

The advanced packaging technology of the double sided die attach using transient liquid phase bonding and soldering has been previously presented in detail [2, 3] (figure 3). The high re-melting temperatures of the formed intermetallics (TLPB and TLPS interfaces) within the assembly allow it to use a slightly modified SAC solder process to attach the TE coolers on top. The thermal buffer modules are finally clamped onto the TECs using a high conducting thermal interface. Well performing thermal interfaces in between IGBT, TEC and buffer are not mandatory (since it can be adjusted by the TEC operation, if within range of performance). But they will increase the system's coefficient of performance and will therefore be of delicate influence referred to the available overload duty cycle and buffer time capability. This includes the thermal interface resistance between heat pipes and the PCM solder as well.

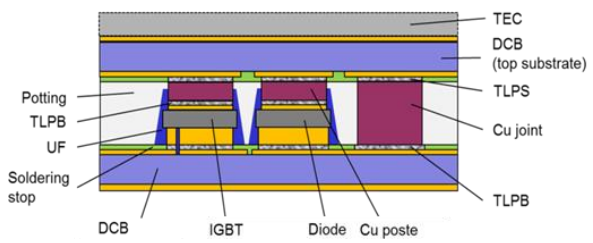


*Figure 3: Joining technology applied in a process hierarchic assembly of the half bridge module*

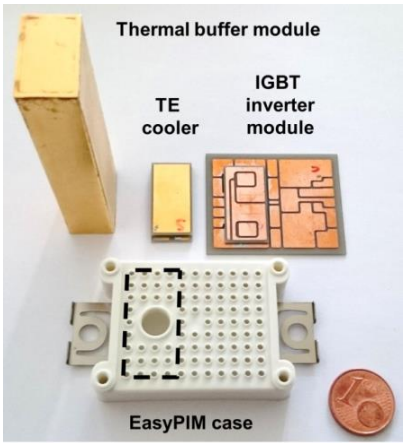


*Figure 4: Modules of the topside thermal cooling concept, inserted into industrial PIM standard casing.*

Therefore, referring to the thermal buffer module assembly, two different coating strategies are pursued allowing and suppressing a firmly bonded contact between buffer casing, heat pipes and solder.

A nickel + gold coating (ENIG) will be used to achieve a good wetting, firmly bonded and therefore thermally well conducting interface. However, we will perform repeated re-melting cycling tests in order to determine thermal performance degradation due to a reformation of the solder's intermetallic structure. From a thermal point of view, the melting point and range must not drift during cycling, since the thermal system is fragile and explicitly designed regarding to the temperature values of solder melting and allowed junction temperature $T_{Melt}$ and $T_{J,max}$ respectively.

The other attempt will consist of only a nickel coating. A subsequent oxidation process (10h @ 200°C, to avoid damage of the water based heat pipes) will form a nickel oxide passivation to allow only a tight fit between solder and casing. This is envisaged to prevent cycling drifts of the solder compound and therefore melting behaviour, but comes with a higher thermal interface resistance.


*Figure 5: Thermal buffer parts (Half-bridge module), cork alike joint of Ni+Au (Var 1) and NiOx (Var 2) coated copper parts.*

The assembly of the buffer modules was done as follows:

1. Milling of the casing parts
2. Ni / Au coating / thermal oxidation treatment
3. (Removing oxide from heat pipes and socket holes)
4. Soldering of the heat pipes
5. Pressing of HP socket into copper shell
6. PCM filling ($Bi_{57}Sn_{42}Ag_1$)
7. Pressing of top socket into filled module
8. SAC solder sealing of the outer joint grooves (since the desired self-sealing by a tight pressing fit could not be achieved reliable due to the tolerances of the low cost milling process).

Note that the heat pipes have to be fixated into the bottom copper socket, since these tend to swim in the PCM solder, when molten. As there are only parts made of copper involved, we expect no reliability issues regarding the thermo-mechanical stability of the thermal buffer modules.

## 3 Attempt for design of the thermal cooling system

In order to successively develop a feasible concept of this ambitious cooling idea, an in depth design study has been performed [1, 2, 3]. This includes simulations on system and sub-system level, thermal characterisation and testing as well as conceptual design studies and estimations. Figure 6 – 9 show a summary of the studies so far.

- We did performance characterisations of the thin TE coolers that were meant to be used in the demonstrator. This was done by using these modules within a small scale cooling scenario and recreating the measured thermal situation within finite element simulations.
- Based on the measured TEC performance data and literature data of the various layers and PCM solder, first system simulations have been performed in order to reveal weak spots and thermal issues like the low thermal heat diffusion during overload and PCM melting, necessity of TEC cooling during the thermal reset phase in order to reflux the stored energy in a controlled manner and the maximum overload duty cycle in order to fully reset the thermal system. This FE analysis has been done in conjunction with equivalent circuit estimations especially referring to an optimal number of TECs and the needed TECs' current.
- To address the problem of the thermal buffer's low thermal diffusivity, a simulation study of different thermal buffer modules has been done, considering thermal conduction enhancing structures like foams or wraps of copper and aluminium and also the inset of heat pipes in various configurations. Regarding the temperature slope during overload, a ranking of these structures has been deducted. A heat pipe's effective thermal conductivity of at least $\lambda_{HP,eff}$ = 10 kW/m/K within a reactor type buffer structure has shown first good and feasible results with a good thermal access to the PCM and therefore only minor overload temperature slopes.
- In order to build this thermal buffer module with respect to the previous simulation results, dedicated heat pipe and thermal buffer characterisations have been done. Already in good agreement with the characterisation data, the simulation models had only to be adjusted slightly regarding melting range and latent heat. The performance of the heat pipes, however has found to be investigated accurately. As COTS parts the performance varies a lot and the first mesh type HPs did not perform sufficiently with only an effective thermal conductivity of $\lambda_{HPmesh,eff}$ = 1.3 kW/m/K.

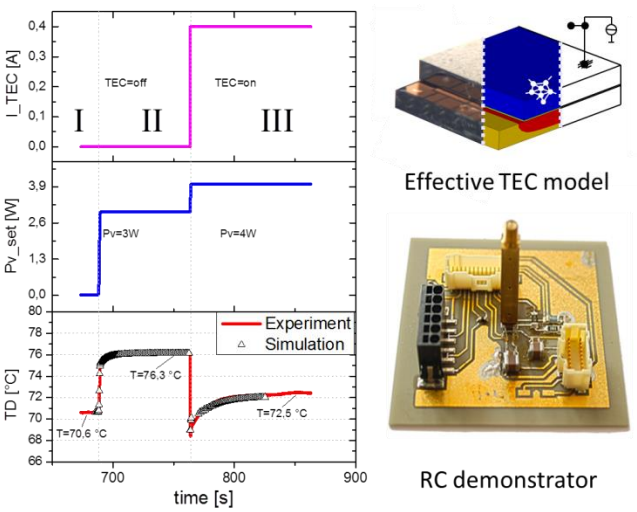


*Figure 6: TEC characterisation and small scale TEC cooling experiment data in good agreement with corresponding FE simulations*

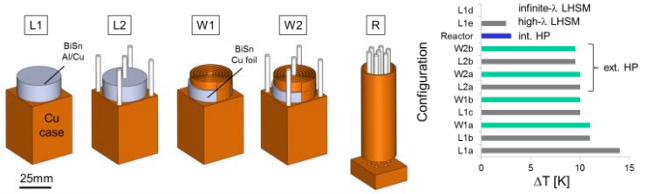


*Figure 7: Temperature slope ranking of PCM buffer concepts using heat pipes and copper/aluminum conductivity enhancing structures*

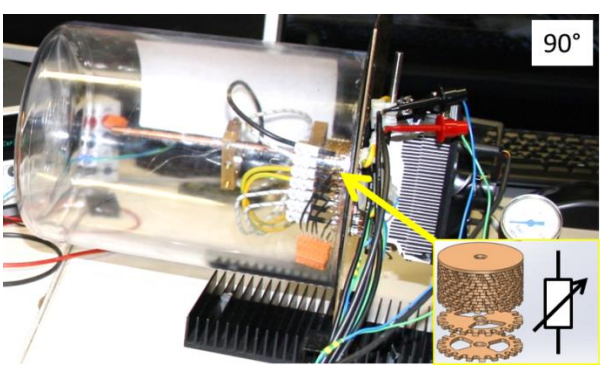


*Figure 8: Tiltable power- and temperature-controlled heater, inserted into an evacuation chamber for heat pipe and thermal buffer testing*

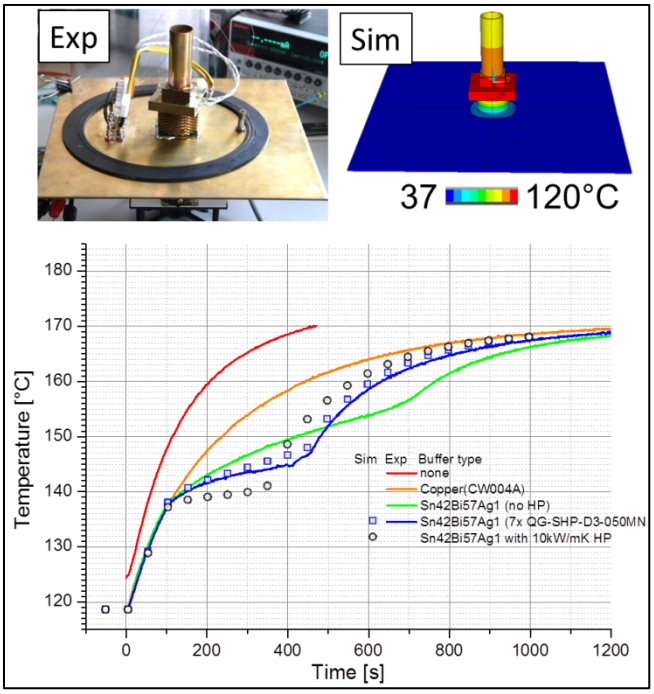


*Figure 9: Measured and simulated temperature response of different thermal buffer types.*

Since it was found that the performance of the buffer diffusion enhancing heat pipes is of great importance, we have replaced the mesh heat pipes with sinter structured HPs, which have a much better performance as shown in figure 10. It can be seen that the heat pipes achieve the conduction demand of $\lambda_{HP,eff}$ ~ 10 kW/m/K within the relevant operation range ($T_{HP}$ = 120°C … 150°C and $P_{HP}$ = 5 … 15 W). This is mainly a result of the sintered wick structures enhancing the capillary performance (driving force of the HP's condensed water reflux) compared to the mesh type HPs. Figure 11 shows the wick structures of the compared 3 mm mesh and sinter heat pipes for the buffer modules.

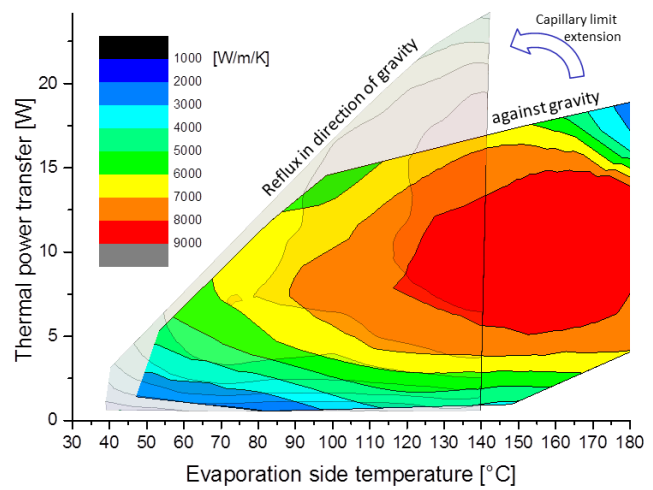


*Figure 10: Effective conductivity of 3mm sinter heat pipes as function of heat power transfer and temperature. The tilt angle extends the conduction performance, depending on the reflux direction in or against gravity.*

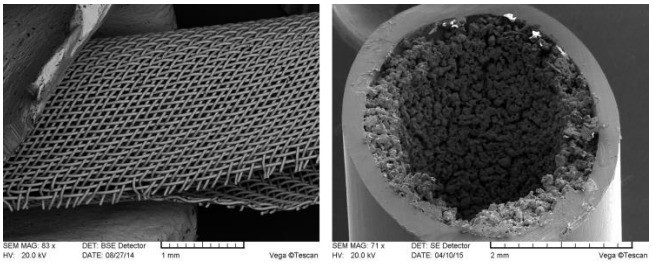

*Figure 11: Wick structures of mesh (left) and sinter (right) heat pipes*

Furthermore, a replacement of the thin film TECs by a better performing thick film TEC with a dedicated design has been done. Figure 12 shows the performance curves and estimated operation range of this TEC for the IGBT half bridge configuration ($P_{J,OL}$ = 16 W, $\Delta T_{TEC}$ = 10 … 20 K).
A complete system experiment including both, thick film TE cooler and phase change latent heat storage module (Half bridge) will be presented in the next chapter, to show the feasibility of the top-sided cooling stack for power electronics.

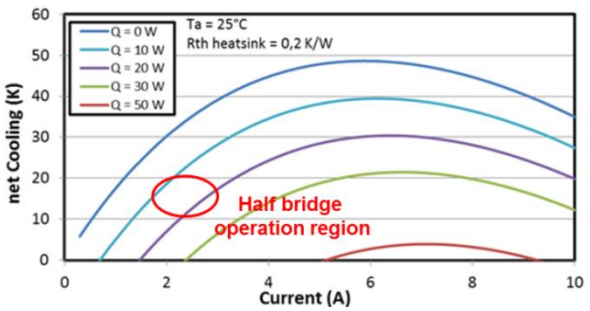


*Figure 12: Measured thick film TEC performance*

## 4 Application and testing

The setup for the cooling scenario under real and specified conditions has been done using the evacuated thermal test stand chamber, which has already been used for the heat pipe and thermal buffer characterisation [3]. It demonstrates the feasible cooling concept of TECs in conjunction with a phase change based temporary and nearly infinite thermal capacitance.

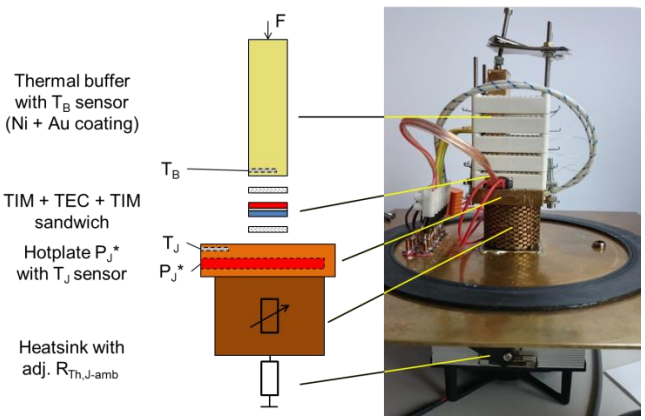


*Figure 13: Setup for electrical overload testing. IGBT power module emulated by heating plate*

The testing setup as shown in figure 13 has been operated with different TEC currents while emulating 110% of the overload power for an IGBT half bridge configuration. The TEC was switched on simultaneously with the switch from normal to overload operation, while the down side cooling path was adjusted accordingly to achieve the specified normal operation junction temperature of 125°C. Table 1 summarises all relevant testing values. The overload duration has been set, according to the junction (hot plate) temperature, to characterise the thermal cooling performance. At the moment when the junction temperature reached the maximal allowed value of $T_{J,max}$ = 130°C, the heating power was set back to normal operation along with a hard TEC switch off, applying no post-cooling.

*Table 1: Half-bridge emulated testing parameters*

| **Quantity** | **Symbol** | **Value** |
|---|---|---|
| Normal power | $P^*_{J,N}$ | 26 W |
| Overload power | $P^*_{J,OL}$ | 16 W |
| TEC current | $I_{TEC}$ | 0,1,2,3,4 A |
| TIM pressure | $P_{TIM}$ | 64 kPa |
| TIM's thermal res. | $R_{TIM}$ *A | 50 mm²K/W |
| Total down side thermal resistance | $R_{Th,\ J\text{-}amb}$ | 3.85 K/W |
| Normal junction temperature | $T_{J,N}$ | 125 °C |
| Overload junction temperature | $T_{J,max}$ | 130 °C |
| Max. $T_J$ increase during overload | $\Delta T_J$ | 5 K |
| Overload time | $t_{OL}$ | $t(T_J < 130°C) - t_0$ |

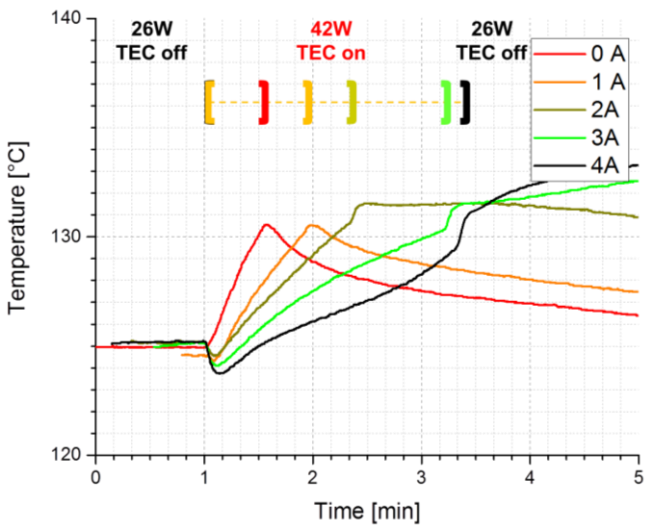


*Figure 14: Junction (hot plate) temperature response using different TEC currents*

The resulting junction temperature and thermal buffer temperature response is shown in figure 14 and 15 respectively. It can be seen that with an increase of the TEC's driving current the temperature slope gets damped during the overload, leading to an extension of available overload time before reaching a junction temperature of $T_J$ = 130°C (figure 16).

A half-bridge overload time of $t_{OL}$ = 130 s could have been achieved with this setup. Considering the rather large thermal capacitance of the test stand and inactive TEC-buffer stack (no top cooling, OL time of $t_{OL,off}$ = 34 s, red curve in figure 14), this would mean an effective top-side cooling performance of 96 s referred to the applicable overload time. This extends the originally 60 s demand of the specification due to some facilitating effects which have not been considered in the design.

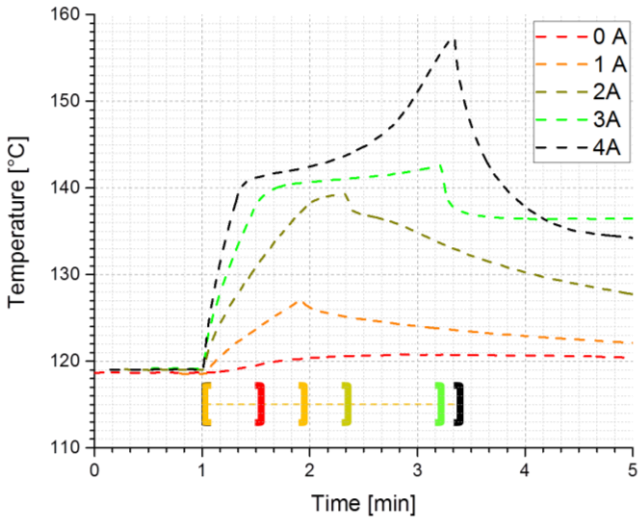


*Figure 15: Thermal buffer (socket) temperature response using different TEC currents*

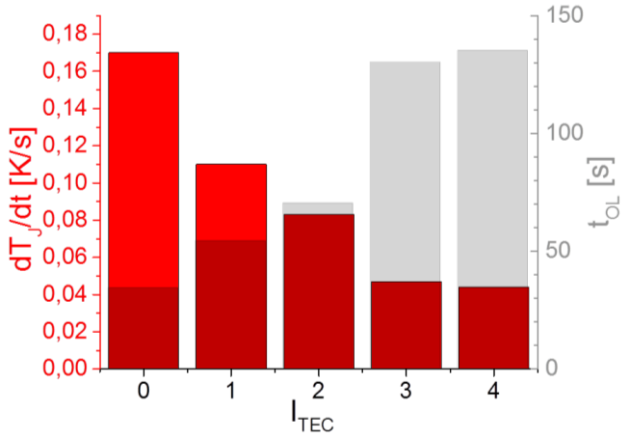


*Figure 16: Comparison of the mean temperature slopes during overload and achieved overload durations while keeping the junction temperature below 130°C.*

One of these is the fact that (besides the conceptual idea of top-sided thermal storage and bottom sided heat removal) a heat rejection to ambient by a top-sided convection of the thermal buffer stack could not be suppressed completely by evacuating the test chamber. Therefore, a normal operation's buffer temperature of $T_B$ = 119°C ensued, providing additional heat storage capability for the overload. Along

with this, additional thermal mass provided by the thermal buffer's copper casing and heat pipes has not been considered in the design and adds up to the PCM capacitance. Since the headroom for the top-side cooling is treated as of minor importance in the first place, the thin film TECs have been replaced by better performing thick film TECs, leading to a COP (@ $I_{TEC}$ = 3A) of 1.2 (instead of 0.875 for the thin film eq. circuit estimation [2]). However, the specified 1 minute of temperature control has been achieved and an adjustment referring to an optimization of the form factor is not foreseen for now.

Also corresponding to the analytical and numerical system analysis in [1, 2] it can be stated that

- There is a minimum of TEC operation power needed to cover both, the (partial) transport of the overload power towards the buffer structure as well as the temperature lifting to initiate the phase change of the $Bi_{57}Sn_{42}Ag_1$ solder at 138°C. In this experiment it can be seen, that at least a TEC current of 2 A is necessary to melt the buffer in time before the junction temperature reaches 130°C.
- The optimal TEC operation is approximately 3 A, since in this case, the complete PCM has been melted (indicated by the slight buffer temperature increase, figure 15, green curve at 3 min) just as the junction temperature exceeds 130°C. A further increase of the TEC current still increased the available overload time duration, but would come with an excess of heat, that has to be stored. A TEC current of $I_{TEC}$ = 4A for example (see figure 16) provided an effective overload time of $t_{OL}$ = 100s but did heat the thermal buffer beyond its phase change. This small bonus (5%) comes with an increase of the time needed to thermally reset the system by approximately 180%. This has to be considered regarding form factor optimisation, a high overload duty cycle and reset ability of the system and thus will be a focus of the on-going work.
- The thermal access provided by the heat pipes used within the thermal buffer is adequate enough. Only a slight temperature increase during the melting process of $\Delta T_B$ = 2 K (green curve, figure 15) can be seen, indicating the desired "post-TEC-sided thermal shortcut" due to the latent heat of the melting PCM. The "reactor type" thermal buffer structure that has been proposed in the preceding FEA studies [2] is therefore proven to be a feasible concept, dealing with the problem of slow heat diffusion during melting of the thermal buffer. This however is the case for the nickel/gold coated thermal buffer where a good thermal and firmly bonded contact between heat pipes and PCM solder is attained. The higher thermal interface resistance of the nickel oxide coated buffers (due to no wetting and form-fit between HPs and PCM) seems to have a minor influence, concluding from simplified melting experiments. This however will be focussed on during the on-going work, along with the investigations regarding the thermal performance degradation under repeated remelting cycles.
- A post-cooling period during the thermal resetting phase is mandatory like it has already been discussed in the thermal system simulations [1, 2]. It can be stated, (figure 14, $I_{TEC}$ = 2,3,4 A) that the stored heat within the thermal buffer tends to "swap" back to the IGBT (hot plate) and thus heats the junction during the relaxation phase to temperatures of over 130°C. To counter this, an active TEC control circuit will be applied to drive the TEC current depending on the junction temperature as well as the buffer temperature, indicating a full reset of the thermal system.

## 5 Conclusions & Outlook

The proposed transient thermal cooling concept of combining thermo-electric coolers and a phase change based thermal buffer has been tested under realistic (for now emulated by a thermal test stand setup) conditions for the first time. The cooling concept has shown to be a feasible tool for novel thermal system designs in electronics, where temporary high thermal loading occurs under low duty cycle conditions. The simulation studies and design, published in previous publications have been experimentally proven to be valid, since the results are in good agreement with the expected thermal performance, derived from the FE system simulations.

The on-going work will focus on the implementation into the IGBT power module while applying a smart TEC control operation, which targets an optimized system coefficient of performance and a proper TEC cooling during the thermal reset phase of the system. Also long-term thermal stability of the PCM solder will be investigated since thermal performance drifts within the fragile thermal system will be critical to the functionality.

## Acknowledgements

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