

Double-Sided Cooling and Transient Thermo-Electrical Management of Silicon on DCB Assemblies for Power Converter Modules: Design, Technology and Test

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Abstract This paper deals with the system design, technology and test of a novel concept of integrating Silicon power dies along with thermo-electric coolers and a phase change heat buffer in order to thermally manage transients occurring during operation. The concept features double-sided cooling as well as new materials and joining technologies to integrate the dies such as transient liquid phase bonding/soldering and sintering. Coupled-field simulations are used to predict thermal performance and are verified by especially designed test stands to very good agreement.

1. Introduction

Novel concepts in power electronics rely heavily on the availability and processability of new materials and packaging technologies to meet the requirements of increasing performance and reliability at lower form factor, weight and cost. Today's main technological route for converter modules is still the power die soldered and wire-bonded to a DCB substrate. New applications or semiconductor technologies like e.g. SiC, however, require enhanced thermal management using standard commercial casings within the same, usually very limited thermal budget.

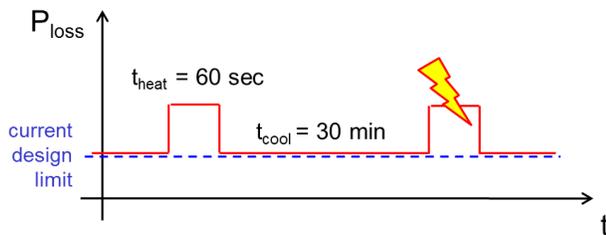


Fig. 1: Loading profile for power converter module. The power transients need to be thermally managed. Details are given in table 1 further below.

This paper deals with such a challenge. As is to be seen in figure 1, the power limit is already reached for a converter module realised in conventional packaging technology. Now, a new load case featuring power transients has to be accommodated by a module of the same footprint.

To solve this, we propose a novel thermal management concept for power electronics enabled by the use of advanced

packaging technologies as well as smart handling of power transients. This concept (figure 2) is exemplified on a typical six-pack converter module for industrial applications (4 kW, 1200 Volts) to be integrated into a standard *easyPIM* casing while being able to cope with overload power pulses:

- The heat generated during the overload pulses is stored in a thermal buffer using the latent heat of a phase transition.
- In order to control the heat flux into and from the buffer, a thermo-electric cooler (TEC) is used.
- The backside of the dies is accessed for additional heat transfer into the buffer, keeping the front side attached to the cold plate via a direct copper bonded substrate (DCB).
- As key enabler to realise this double-sided cooling concept thermally and mechanically, high performing and reliable packaging technologies are needed allowing sequential processing of a multi-chip module as well as high-voltage capability. We have tackled this issue by transient liquid phase bonding and soldering (TLPB/S) using the intermetallics of the Cu-Sn system, increased spacing and encapsulation.

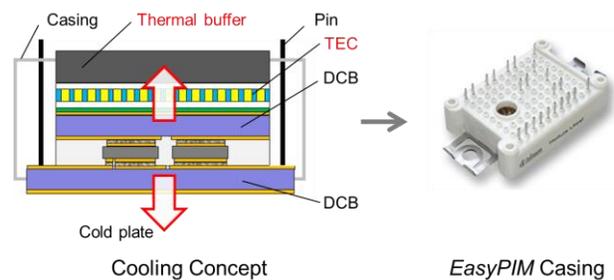


Fig. 2: Schematic of the targeted packaging concept.

This design (for a more detailed exposition about general feasibility see [1, 2]), allows a very compact architecture, having the advantage of not needing to attach the backside of the chips via a large copper clip to the front cold plate which is also a delicate undertaking with respect to precision, thermo-mechanics and customer acceptance.

All this calls for a system approach centred on technology development using design by Finite Element (FE) simulations as well as experimental verification at all stages and for all parameters of interest.

For reference, the specifications and overload ratings used for this work are summarised in table 1 and figure 1.

Table 1: *Specifications*

Quantity	Symbol	Value
Total normal power of module	$P_{N,tot}$	71.04 W
Total overload power of module	$P_{OL,tot}$	43.02 W
Normal power per IGBT	$P_{N,IGBT}$	10.12 W
Overload power per IGBT	$P_{OL,IGBT}$	6.27 W
Normal power per Diode	$P_{N,Diode}$	1.72 W
Overload power per Diode	$P_{OL,Diode}$	0.90 W
Overload time	t_{OL}	60 s
Normal junction temperature	T_J	125 °C
Overload junction temperature	$T_{J,max}$	130 °C
Max. T_J increase during overload	ΔT_J	5 K
Heat transfer coeff. cold plate	h	1805 W/m ² /K
Max ambient temperature	T_{amb}	70 °C

There is one important boundary condition about the maximum allowed temperature on the dies: $T_{J,max} < 130$ °C. With a normal operation temperature of $T_J = 125$ °C, this means that the maximum temperature rise is $\Delta T_J = 5$ K. The cold plate is designed to assure this under normal operation, featuring a heat transfer coefficient $h = 1805$ W/m²/K at $T_{amb} = 70$ °C. Under overload conditions, this is the target value for buffer and TEC performance. The time interval between the overload cases, which is always $t > t_{OL} = 30$ mins, can be used for thermal relaxation. This is one of the prerequisites for the proposed concept.

Buffering thermal energy by exploiting the latent heat during phase change of a phase change material (PCM) has recently attracted renewed attention, not only for space missions [3], but also for thermal management of electronic circuits [4-9]. Here, a huge problem which needs addressing is the homogeneous heating up of the PCM. TEC-assisted cooling of hot spots on chip level has led to many discussions [10, 11], whereas it rarely is found in power electronics due to the low coefficient of performance. In combination, both elements could be used to devise a smart cooling system in that the heat flow into and out of the buffer is controlled by the TEC.

Obviously there is a comment on cost. The authors are aware of the fact that this solution has its price. However, for this special application and loading situation a proof of concept is presented by a system approach, including many elements that could spin off into other areas of power packaging in the future.

2. Analytical Model of TEC-Assisted Thermal Buffer

In order to perform first estimations of the thermal system, simplified and generalized equivalent circuit calculations have been done. As the TE coolers will control the temperatures and melting process, dimensioning (number of TE legs/modules) and needed driving current are of major importance for the system design. These are calculated as well as derived values like the total heating power that has to be stored by the thermal buffer, thus defining the needed volume of the PCM.

The TEC-PCM cooling layer stack and the thermal equivalent circuit are shown in figure 3 with corresponding symbols summarized in table 2.

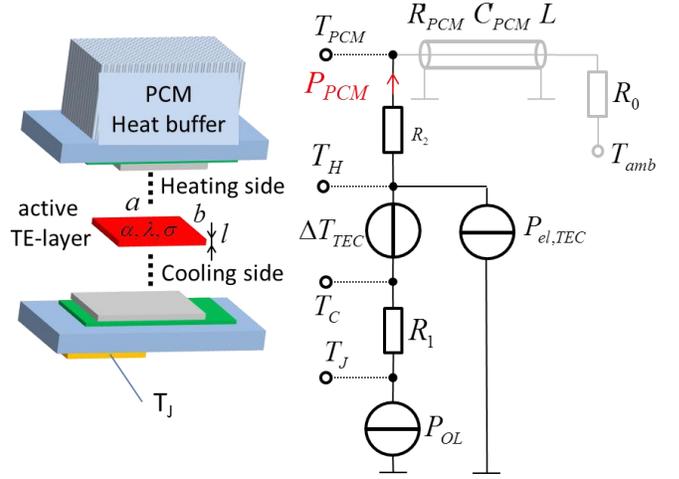


Fig. 3: *Thermal equivalent circuit of a transient TEC-assisted latent heat cooling system.*

Table 2: *Symbols and description*

a, b, l, N_{TEC}	Dimensions and number of the effective TE layers
α, λ, σ	Seebeck coefficient, thermal conductivity and el. resistivity of the TE layer
$T_C, T_H, \Delta T_{TEC}, P_{el,TEC}$	TEC's cold and hot side temperature, temperature difference and power loss of the TEC
T_J, P_{OL}	IGBT Junction temperature and TEC-related overload power, that has to be soaked
R_1	Cumulative thermal resistance of the layer structure between hot spot and TEC
R_2	Cumulative thermal resistance of the layer structure between TEC and PCM buffer
R'_{PCM}, C'_{PCM}	Thermal Resistance and capacitance per unit length of the LHSM buffer
T_{PCM}, T_m	Temperature of the buffer and PCM's melting point
L, R_0	Length and heat sink resistance of the thermal buffer
	* Values referred to one TEC or TE block $C_{PCM} = C_{PCM,tot} / N_{TEC}$ $P_{OL} = P_{OL,tot} / N_{TEC}$

As the thermal buffer system has the task to soak the thermal overload power of the hot spot while keeping the temperature constant or at least below $T_{J,max} = 130$ °C, $P_{OL,tot}$ and $T_{J,max}$ are fixed system boundary conditions. To calculate the required TEC current as a first design point value, the type of transmission line transient behavior of the PCM buffer is ignored, assuming a perfect thermal conductivity. Also additional overload heat flow into the bottom cold plate upon

$\Delta T_J = 5$ K could be found, reducing the overload power buffering demand by at least $\Delta P = 5$ W. This is not taken into account in the equations below, thus providing a factor of safety for the calculations of I_{TEC} and N_{TEC} .

As can be derived from thermo-electric theory [12-16], the net cooling ΔT_{TEC} of the TE layer is given as

$$\begin{aligned} \Delta T_{TEC} = T_H - T_C &= \frac{\rho^2 I^2 + 2ablP_{OL} - 2abl\alpha(T_C + \Delta T_{TEC})}{2ab(-\alpha I - ab\lambda)} \\ &= \frac{\rho^2 I^2 + 2ablP_{OL} - 2abl\alpha T_C}{-2abab\lambda} \end{aligned} \quad (1)$$

With $T_{PCM} = T_m$ and T_J given (PCM's melting temperature and IGBT junction temperature during overload operation) the following relations of the network read as follows:

$$\begin{aligned} T_C &= T_{J,max} - R_1 P_{OL} \\ T_H &= T_m + R_2 (P_{OL} + P_{el,TEC}) \\ P_{el,TEC} &= UI = \frac{\rho l}{ab} I^2 + \alpha \Delta T_{TEC} \end{aligned} \quad (2)$$

Inserting (2) into (1) yields equation (3), the solution of which is the TEC current needed for the required cooling.

$$\begin{aligned} I^3 + AI^2 + BI + C &= 0 \\ A &= \frac{-2abR_2(\alpha\lambda + \alpha^2(T_{J,max} - R_1P_{OL})) - \sigma}{\alpha R_2 \sigma} \\ B &= \frac{2ab(P_{OL}(R_2 - R_1) + T_{J,max})}{R_2 \sigma} \\ C &= \frac{2a^2b^2\lambda(T_{J,max} - T_m - P_{OL}(R_2 + R_1))}{\alpha R_2 \sigma^2} - \frac{2abP_{OL}}{\alpha R_2 \sigma} \end{aligned} \quad (3)$$

Referring to the system's and TEC's coefficient of performance (COP) an optimum number of TEC components exists, minimizing the TEC's heat loss per pumped power. To reduce the needed PCM buffer volume, this should be taken into account.

Table 3: Thermal resistance values for schematic in figure 4.

	Notation	Thck. [mm]	Area [mm ²]	l [W/m/K]	R [K/mW]
1	Cu, 2	10.000	25x28	391	3.65E-05
2	TiM	0.020	3.364 x 3.388	5	3.51E-04
3	Si, TEC, 2	0.525	3.364 x 3.388	98	4.70E-04
4	Si, TEC, 1	0.525	3.364 x 4.248	98	3.75E-04
5	SAC	0.030	3.364 x 4.248	60	3.50E-05
6	Cu, 1	0.127	25.58 x 28.54	391	4.45E-07
7	AlN	0.600	25.58 x 28.54	180	4.57E-06
8	TLPS	0.095	5.67 x 5.07	122	2.71E-05
9	Cu-poste	0.300	5.67 x 5.07	391	2.67E-05
10	TLPB	0.010	5.67 x 5.07	43	8.09E-06

For the IGBT module the thermal resistances R_1 and R_2 are approximated by the thermal resistance network of the double-sided cooling structure shown in figure 4 and listed in table 3.

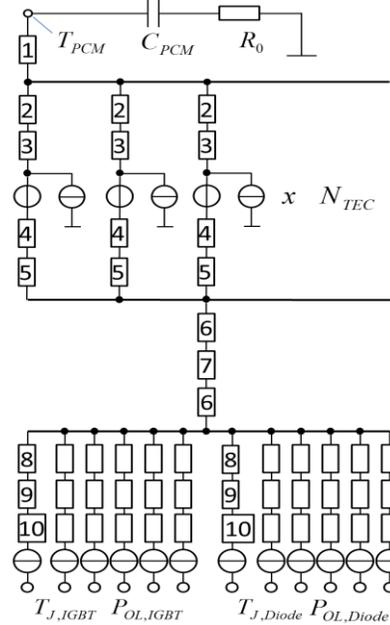


Fig. 4: Thermal resistance structure of the TEC-PCM thermal buffer on top of the power converter.

The whole resistance stack is now simplified to the TEC-related thermal resistances R_1 and R_2 (see figure 3), neglecting spreading resistances and merging diodes and IGBTs by using the fact, that $P_{OL,Diode} = 0.1435 P_{OL,IGBT}$.

$$\begin{aligned} R_1 &= R_{Si,TEC,1} + R_{SAC} + N_{TEC} \left(2R_{Cu,1} + R_{AlN} + \frac{R_{TLPS} + R_{Cu-poste} + R_{TLPB}}{6 \cdot 1.1435} \right) \\ R_2 &= R_{Si,TEC,2} + R_{TiM} + N_{TEC} R_{Cu,2} \end{aligned} \quad (4)$$

The TEC-related overload power (thermal power each TEC has to pump) is given in equation 5.

$$P_{OL} = \frac{P_{OL,tot}}{N_{TEC}} = \frac{6(P_{OL,Diode} + P_{OL,IGBT})}{N_{TEC}} = \frac{6.861 \cdot P_{OL,IGBT}}{N_{TEC}} \quad (5)$$

For the active TEC layer, the use of thin film TE components was considered with data taken from the manufacturer's data sheet (later, in section 3, we will generate a compact model ourselves).

As for the overload operation and for a PCM of eutectic BiSn, the TECs will have to maintain a ΔT of at least 8 K ($T_m = 138^\circ\text{C}$, $T_{J,max} = 130^\circ\text{C}$) while pumping the heat load of $P_{OL,tot} = 43.02$ W. As shown in figure 5, a minimum number of ten and an optimum number of $N_{TEC} = 38$ thin film TE coolers are obtained, leading to TEC currents of $I_{TEC} = 0.9$ A and 0.265 and a total heat power (converter overload + TEC's heat loss) of $P_{PCM} = 120$ W and 69.1 W respectively.

Due to the availability of thin film modules, a small number of 12 TECs was chosen for the TE simulations, leading to the buffer heat overload of $P_{PCM} = 93$ W and the heating energy of $Q_{OL} = 5.58$ kJ which has to be soaked by the thermal buffer during the overload of $t_{OL} = 60$ s. For the BiSn

PCM (enthalpy of fusion of $M = 383 \text{ J/cm}^3$) a volume of around $V_{PCM} = 14.4 \text{ cm}^3$ would be sufficient to cover this thermal capacity demand.

a [mm]	b [mm]	l [mm]	ρ [mW/mm]	λ [mW/mm/K]	α [mV/K]	T_1 [°C]	T_m [°C]
3.364	3.388	0.036	225	0.43875	0.2821	130	138

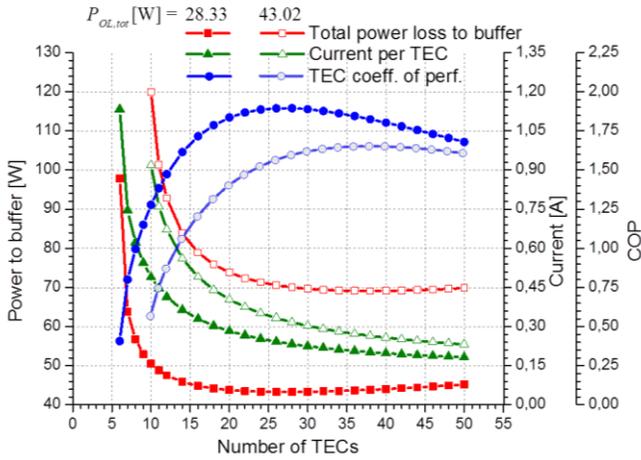


Fig. 5: TEC current, system COP and power loss as a function of the number of thin film TECs given for two relevant power ratings (see text).

Later in the paper, see section 8, as a first fully functional demonstrator will be built featuring only six TECs. This demo will be capable of an overload case of $P_{OL,tot} = 28.33 \text{ W} = 6 P_{TEC}$, ($P_{PCM} = 98 \text{ W}$ and 6 TECs @ $I_{TEC} = 1.13 \text{ A}$). Hence the second set of curves in figure 5.

3. Compact TEC FE-Model

To reduce the complexity of the system FE models, a compact model for the TEC has to be generated, using effective material data and only one single TE layer emulating the thermo-electric behavior of the complete TEC structure, the TE-junctions, metallization layers and thermal interfaces. This method has been described in [1, 2] and is depicted in figure 6 for the considered thin film TEC. It consists in calibrating the model first against manufacturer's data, then against own precision measurements performed with simplified boundary conditions. A set of effective values α, λ, σ was thus derived for the compact model.

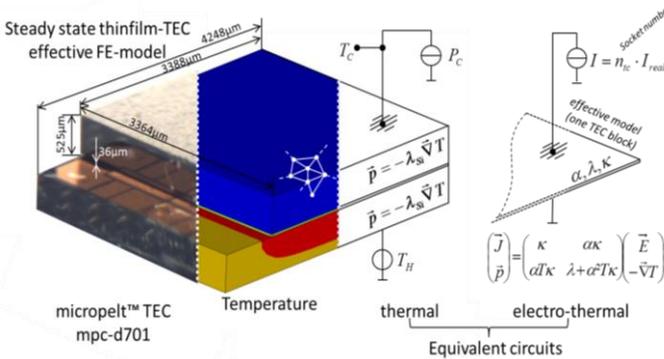


Fig. 6: Generation of compact, coupled field TE-model by FE-simulation using effective properties for thin film TEC [2].

To validate this compact model, and to refine it if necessary, TEC testing under real transient overload conditions was carried out.

4. Experimental Validation for TEC

In order to validate/adjust the transient TE-simulation models for the overload case by realistic measurements on module level, a reduced complexity (R.C.) test device has been realized employing standard joining materials and technology (see figure 7).

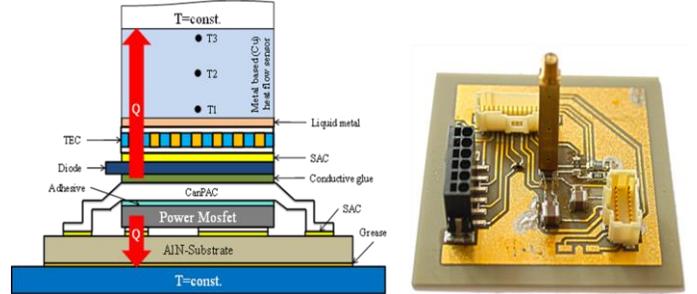


Fig. 7: RC device schematic and assembled module. Top and bottom cold plate are not depicted.

The demonstrator, which is to be understood as a miniature version of the power module, consists of a heat source (packaged MOSFET transistor), one TE module and a thermal resistor as heat flow sensor on top. Several temperature sensors, including a diode (bare die) sandwiched between the MOSFET and TEC and the heat flow sensor measure the thermal state of the system. The device is put in between two liquid-cooled cold plates, thus keeping the temperature at the top (thermal resistor) and bottom (ceramic substrate) at the same value over time. Both the power dissipation in the transistor and the pumping power of the TE cooler can be controlled. Static operation as well as transients can be realized. For a detailed description see [1].

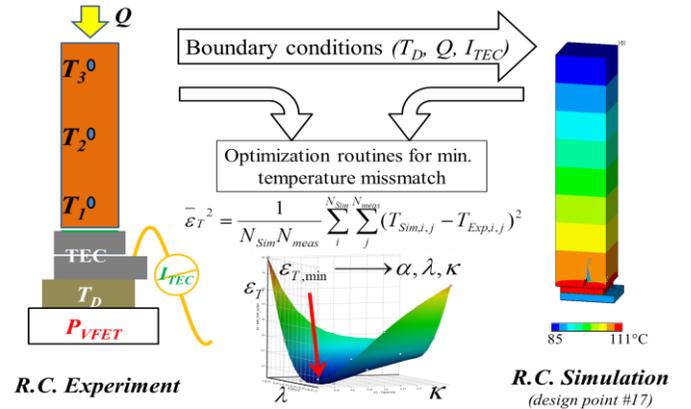


Fig. 8: Principle of the TEC model optimization using the R.C. demonstrator.

Figure 8 shows the principle of the TEC data optimization, using the measured temperature and power data of the R.C. demo experiment as input data for an electro-thermal transient simulation. The temperature data of the heat flow sensor are

used to fit the TEC-model performance by means of least square optimization.

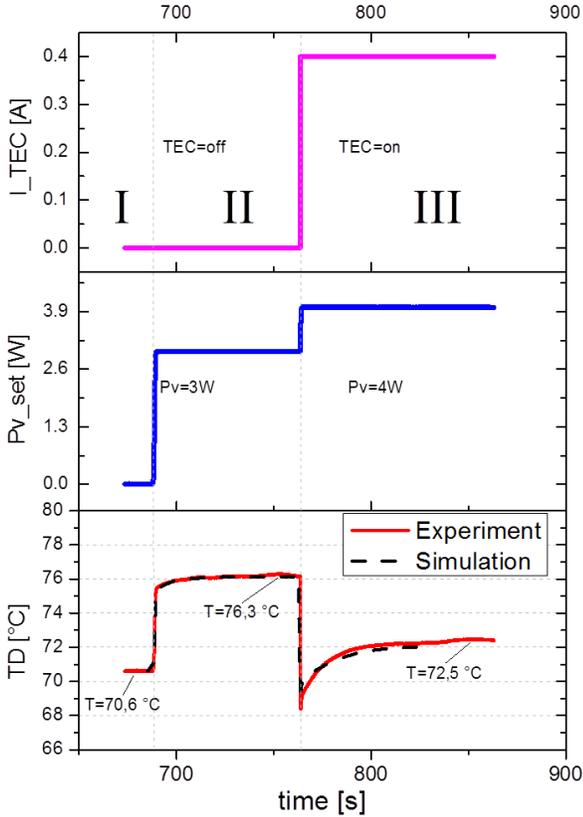


Fig. 9: Very good agreement between experiment and simulation. The given overload case (25%, $P = 3W \rightarrow 4W$) mimics the real situation in the full power module qualitatively.

Figure 9 shows the excellent agreement between the effective model and the transient measurements on the RC tester. Since only minor scaling factors ($c_{\lambda} = 1.0015$, $c_{\rho} = 1.000074$ and $c_{\alpha} = 1.082$) had to be applied, accounting for less than 10 % deviation, the compact model proved itself, and sample variation and drifts due to the soldering process can be stated to be negligible.

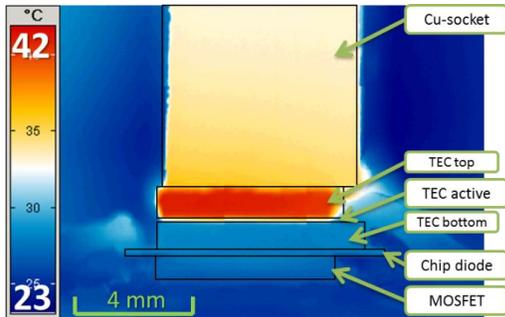


Fig. 10: IR image of RC-demo activated TEC. Note the cooling effect of the TEC on the FET.

Also note the cooling effect by the TEC on the die (also seen in figure 10 by IR-thermography) as well as the long equilibration time (exponential thermal equilibration

behaviour) after switching a large thermal mass (the resistor incl. part of the cold plate) to the die by activating the TEC.

So it has been shown that T_J can be kept constant or reduced even under additional realistic overloading plus the losses caused by TEC heat pumping.

As the thermal capacity of the very thin ($\sim 36\mu\text{m}$) active layer of the TECs is only of minor impact to the transient TEC behavior, well known literature data for density and specific heat of the adjacent silicon substrates are used. The optimized thermo-electric data that was found is listed in table 4.

Table 4: Refined temperature-dependent electro-thermal data of a R.C. demo TEC mpc-d701

T [°C]	3	25	33	60	80	120
λ [mW/mmK]	0.394	0.398	0.402	0.411	0.422	0.422
ρ [$\mu\Omega\text{m}$]	216	216	216	216	216	216
α [$\mu\text{V/K}$]	285.4	287.3	288.1	290.6	293.8	293.8

Note, as this is an effective model, the data differs from the Bi_2Te_3 values given in the literature, depending on the number of TE couples and filling factor of the TE structure.

With the TE-model well calibrated and tested we can now proceed to the system simulation including the buffer.

5. Material Data for Thermal Buffer Model

The thermal buffer will need two special features: The PCM to buffer the heat through the latent heat while undergoing phase change, and materials to enhance heat transfer into the PCM. As we will see, heat pipes (HP) are well suited to do this as they are available today as COTS parts in various shapes and power ratings [17-19].

The choice of the PCM is important, as it must fit the operation conditions. As seen from table 5, only (eutectic) alloys are eligible for our purposes. Although waxes are already used in thermal buffer devices (see e.g. [3]), they are ruled out by their too low melting temperature. Pure metals cannot be used as they are too high melting. As material of choice eutectic BiSn42 was chosen with a $T_m = 138^\circ\text{C}$ slightly higher as our maximum allowed $T_{J,max} = 130^\circ\text{C}$, leaving a temperature delta small enough to be exploited by the TEC and one large enough to leave scope for tolerances.

Table 5: Criteria for choice of PCM

Material	Wax	Metal	Eut. Alloy
Pro	- high M - th.dyn. stable - inexpensive - experience	- high λ - high M	- medium λ - medium M - medium T_m
Con	- low T_m - very low λ	- high T_m	- formation of IMC

Thermal and thermo-electric material data used in the simulations is given in table 6. Particle or volume percentage analyses have been carried out on the TLPB and TLPS cross-sections to determine effective material data of these joints. The data of the heat pipes has been approximated using the given typical thermal resistance within the datasheet and are also discussed in [20].

Since most of the PCM's literature lacks exact $c_p(T)$ distribution data, a simplified *peak type* $c_p(T)$ model has been applied in analogy to enthalpy based model descriptions [21].

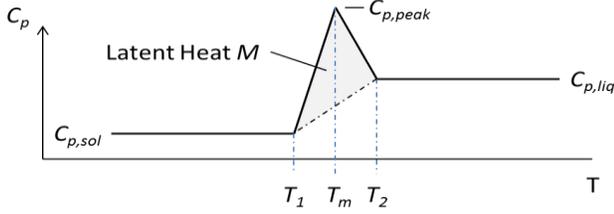


Fig. 11: Enthalpy of fusion M of PCM integrated into the specific heat values using a simplified “peak type” $c_p(T)$ distribution.

$$c_{p,peak} = \frac{2M}{T_2 - T_1} + \frac{(c_{p,sol} + c_{p,liq})}{2} \quad T_m = \frac{T_1 + T_2}{2} \quad (4)$$

Table 6: Thermal material data @ RT, Units: mm-t-s-A-K

Material	Th. Cond. [mW/mm/K]	Density [t/mm ³]	Specific heat [mJ/t/K]
Si	148	2.33E-9	712E6
TLPB (eff.)	43	8.53E-9	302E6
TLPS (eff.)	122.1	8.42E-9	310.7E6
Cu	398	8.92E-9	385E6
Al	237	2.7E-9	897E6
AlN	285	3.26E-9	740E6
HP (eff.)	10k (100k) [20]	-	-
TIM TEC-PCM	5	-	-
PCM: BiSn42	19 (sol.) ~15 (liq.) [22, 23]	8.56E-9 [22]	$c_{sol}= 167E6$ $c_{liq}= 201E6$ $T_1= 137^\circ\text{C}$ $T_2= 139^\circ\text{C}$ $M= 44.8E9 \text{ mJ/t}$ [22]

The specific heat's peak value is defined by the latent heat of fusion M , the specific heat in the solid and liquid state ($c_{p,sol}$ and $c_{p,liq}$) as well as an melting temperature range T_2-T_1 (equation 4) introduced for computational reasons.

6. Architectural Concept of Thermal Buffer

The requirement to the TEC assisted thermal buffer is to provide a near-zero (referred to overload power) thermal resistance and literally soak all the overload heat, inducing no temperature increase. In order to develop guidelines and design rules, as well as to show the feasibility of the cooling concept, electro-thermal transient finite element simulations have been performed.

Compared to the 1-D analytical estimation (section 2), first FE-simulations using a perfectly conducting thermal buffer reproduced exactly the analytical prediction, thus validating the models. However, upon application of realistic material data, three crucial points emerged (figure 12):

- Insufficient diffusivity of the thermal buffer, mainly along the vertical, leading to a non-uniform melting process and thus unwanted and considerable temperature increase of T_H and T_J (i.e. the TEC's heating side and IGBT junction temperature) $\rightarrow \Delta T_1$
- “Back-swapping” of the stored energy if there is no TEC current applied during the relaxation period ($I_{TEC} = 0A$) to control the heat flux. As a consequence, the buffer heats up the IGBT. $\rightarrow \Delta T_2$
- The relaxation time or performance of the buffer has to be appropriately dimensioned in that the thermal system can be fully reset to normal operational conditions. Otherwise the stored energy of the system rises with each overload cycle $\rightarrow \Delta T_3$.

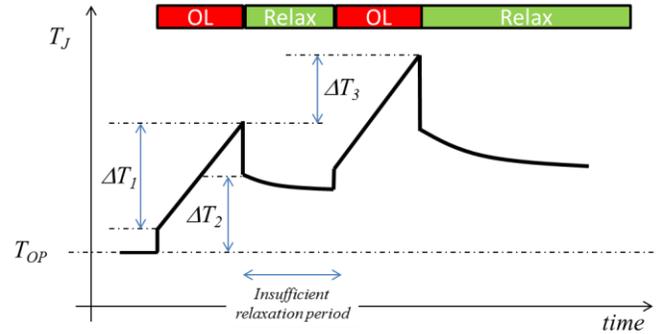


Fig. 12: IGBT temperature increase, due to problematic thermal effects of the cooling concept

To address the most critical point, insufficient diffusivity, several buffer concepts with copper/aluminum foam- and wrap-type conductivity enhancements, some also in combination with heat pipes, have been studied and assessed w.r.t. ΔT_J . These different concepts are shown in figure 13.

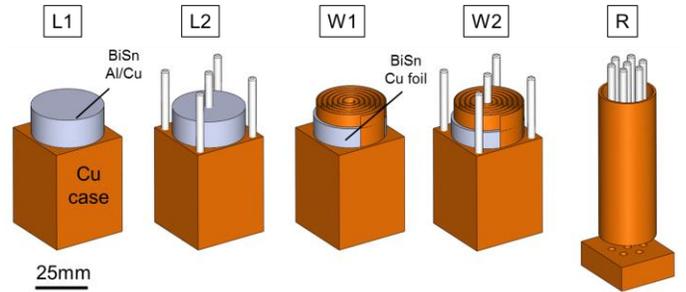


Fig. 13: PCM buffer concepts using heat pipes and copper/aluminum conductivity enhancing structures:

- L1 foam/sponge type PCM compound
- L2 L1 with heat pipes put into the case
- W1 Wrap of copper/Bi₅₈Sn₄₂ foil as PCM comp.
- W2 W1 with heat pipes put into the case
- R “Reactor” type

As can be seen in table 7, effective diffusivity data has been calculated to mimic the situation of the phase change material within a Al or Cu foam matrix to enhance isotropic heat transfer across the buffer (lumped concepts L) volume or

wrap type architectures supposed to mainly boost heat transfer in axial direction.

In figure 14, a ranking of the configurations is given w.r.t. the target value ΔT_I . As is apparent, wraps to not really outperform foam enhancements, even external heat pipes do not significantly homogenize the temperature along the buffer.

Table 7: Effective material data used for FE simulations.

Concepts	PCM compound (%Vol.)			PCM Th. cond. λ [mW/mm/K]	Dens. ρ [t/mm ³]	Spec. heat. C_p [mJ/t/K]	ΔT_I [K]	
	Bi Sn	Al	Cu					
L1a	100	0	0	19 (sol.) ~15 (liq.)	8.56 E-9	$c_{sol}= 167E6$ $c_{liq}= 201E6$ $T_1= 137^\circ C$ $T_2= 139^\circ C$ $M= 44.8E9$ mJ/t	14	
L1b	65	35	0	95 (sol.) 93 (liq.) +	6.51 E-9	$c_{sol}= 423E6$ $c_{liq}= 445E6$ $T_1= 137^\circ C$ $T_2= 139^\circ C$ $M= 28.8E9$ mJ/t	11	
L1c	65	0	35	152 (sol.) 149 (liq.) ++	8.69 E-9	$c_{sol}= 243E6$ $c_{liq}= 265E6$ $T_1= 137^\circ C$ $T_2= 139^\circ C$ $M= 28.8E9$ mJ/t	10	
L1d Ideal	100	-	-	∞	#	*	0	
L1e 20x λ	65	-	-	380 (sol.) 300 (liq.)	##	**	2.5	
W1a	65	35	0	ϕ z : 95 (sol.) 93 (liq.) r : 28 (sol.) 22.3 (liq.) +++	##	**	11	
W1b	65	0	35	ϕ z : 152 (sol.) 149 (liq.) r : 28.5 (sol.) 22.6 (liq.) ++++	###	***	10	
L2a	65	35	0	+	##	**	10	
L2b	65	0	35	++	###	***	9.5	
W2a	65	35	0	+++	##	**	10	
W2b	65	0	35	++++	###	***	9.5	
R	85	real material model						3

The real bottleneck is the low thermal conductivity of the PCM itself. This is seen from the first two configurations where λ is first set to a very high value (L1d), then to the value of copper (L1e). As this is purely imaginary, the first realistic configuration is the “reactor” type architecture. Therefore, it is looked into in detail in the following.

In order to do that, we now draw upon all previously obtained knowledge and build a system model consisting of the top DCB, the diodes and IGBTs, the TECs and the buffer with detailed internal architecture (see figure 15). The heat path through the bottom DCB and the cold plate is modeled implicitly by a boundary condition, as this path has not changed. A graphical depiction of the transient loading

conditions for IGBTs, diodes and TECs is also given below in figure 15. To enhance also radial heat transfer, the heat pipes are packed closely together.

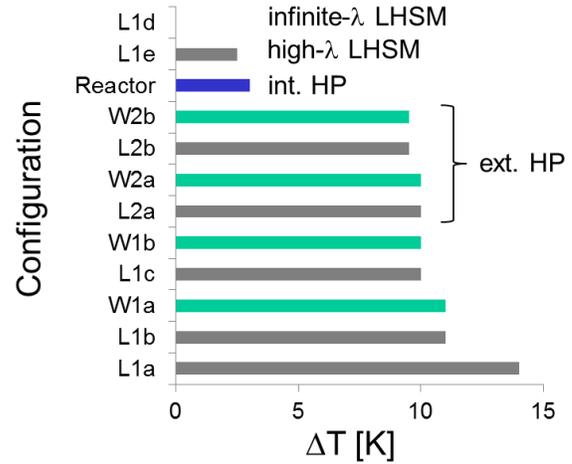


Fig. 14: Ranking of simulated configurations w.r.t. ΔT_I above T_{liq} . The first realistic option is the “reactor” type with internal heat pipes (HP).

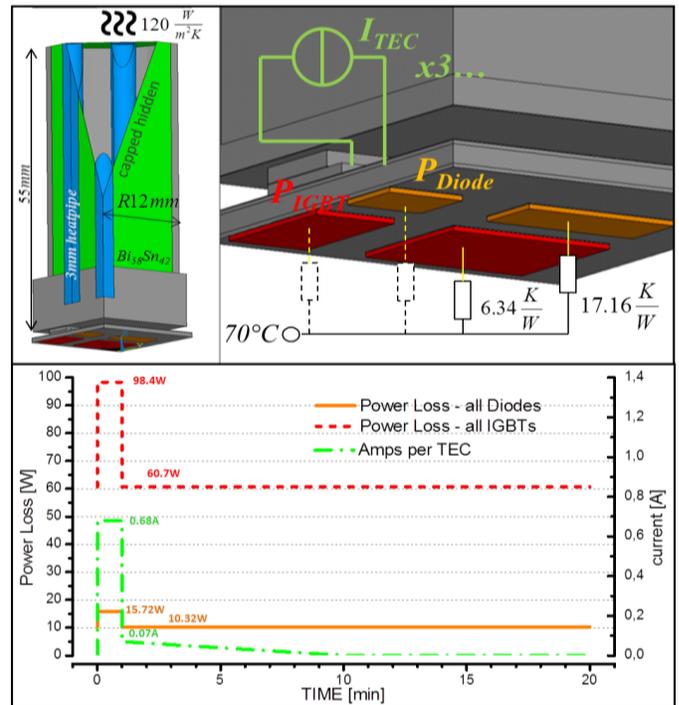


Fig. 15: Transient electro-thermal FE model and BC of the thermal buffer system for the IGBT power device (quarter symmetry, “reactor” type model).

The following design and loading parameter were used for the reactor type model:

- Diffusion enhancement through seven 50 mm long heat pipes (18 W power rating, 3 mm diameter) within the BiSn PCM buffer.
- A buffer’s relaxation phase using a de-ramping of the TEC current from $I_{TEC} = 70$ mA down to zero during $t = 9$ min (see figure 15).

- A total relaxation period of $t = 20$ min, to provide sufficient time to reset the thermal system (figure 15). As shown in figure 16, a thermal reset of the system can already be stated after around $t_{res} = 15$ min.

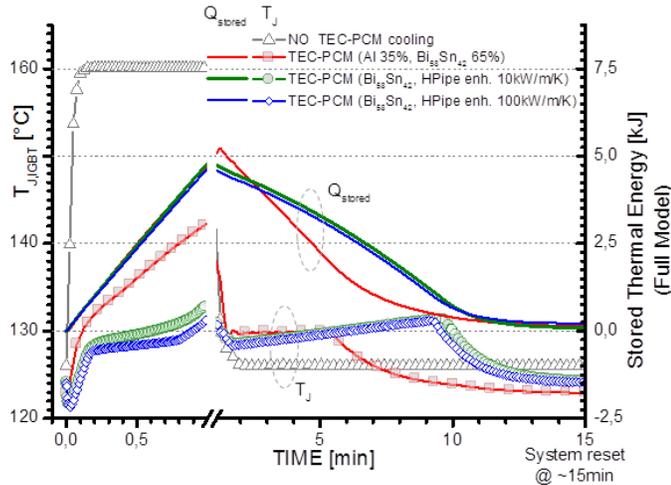


Fig. 16: Simulation results: IGBT Junction temperature and stored thermal energy for various configurations.

Figure 16 shows that in comparison to no-TEC-PCM cooling (huge thermal runaway) and configuration L1b the junction temperature can indeed be maintained at around the required $T_j = 130$ °C to within $\Delta T = 2$ K. So our system works as desired.

Referring to the thermal energy reflux into the bottom cold plate and top-side PCM heat rejection, a thermal system reset can be reported after around $t_{res} = 15$ min (figure 16). Also, during relaxation, a temperature increase can be stated which is due to the de-ramped post-cooling of the TECs.

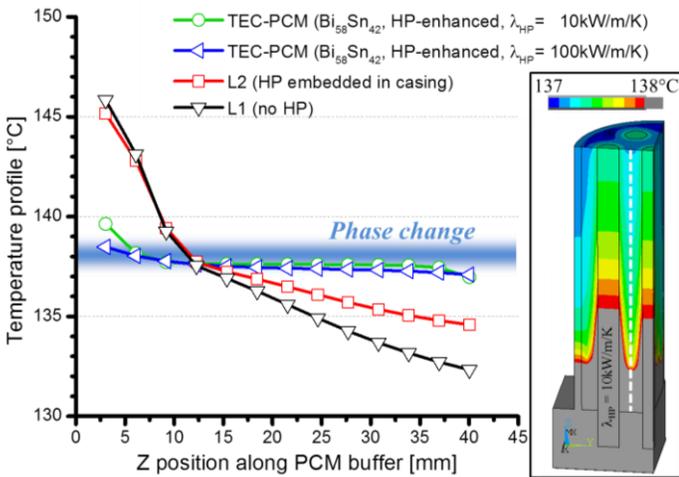


Fig. 17: Temperature profiles of the buffer concepts, middle of heat buffer (lumped models) or in between of two heat pipes (reactor type concept) at $t_{OL} = 30$ s. The inset shows the homogenizing effect of the heat pipe.

A more detailed control of the TEC's current could provide a more linearized trend of $T_{J,IGBT}$ (@130°C) and will

be part of further investigations and simulations, following also the goal of a 100% bottom side reflux period.

It is instructive to look for the reasons behind this behavior. In figure 17 the temperature along the vertical between two heat pipes in the PCM is plotted. As can be seen, the heat pipes really manage to toggle the temperature to the melting point of the eutectic alloy all along the vertical axis as required. Other configurations show non-homogeneous melting resulting in a temperature increase before the end of the overload period.

However, it is not only vertical conductivity: Further enhancement beyond $\lambda_{HP} = 10$ KW/mK does not bring any benefit, whereas placing the HP in the centre as in a reactor type configuration also circumvents the problem of low radial conductivity.

Summarizing the design rules, we can state:

- $N_{TEC} = 12$. More would be desirable to increase the COP.
- PCM BiSn42 ideally suited, with $M = 383$ J/cm³ and $T_m = 138$ °C. To buffer the $P_{OL} = 5.5$ kJ, $V_{PCM} > 15$ cm³.
- Heat pipes are mandatory here to decisively enhance thermal conduction. Other passive options are not sufficient.
- Post-cooling: After loading a sufficient time of thermal recovery has to be taken into account to drain the heat flow back into the bottom cold plate.

With the feasibility of this concept proven, one can proceed to further design of the power module.

7. Power Module Design for NTEC = 6

A first fully functional demonstrator is to serve as proof of concept using the buffer, TECs and advanced joining technologies for sequential assembly to fit into the foreseen *easyPIM* casing. Figure 18 depicts an exploded view of the targeted module including the properly layouted and functional designs for the top and bottom DCBs

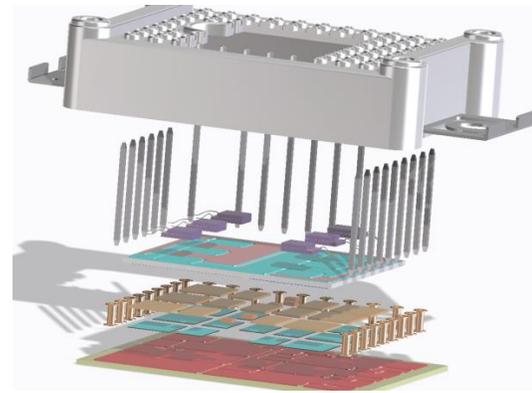


Fig 18: Exploded CAD view of the targeted module. The hole in the top provides space for the buffer.

The layout of the bottom DCB enables the assembly of six IGBTs and six diodes. The layout of the upper DCB provides space for mounting six TECs above each aggregate (IGBT & Diode) and wire bonding pads for the power supply of the TECs. From the top of the TECs the heat is to flow into the top-mounted thermal buffer.

8. Power Module Thermal System Simulation for $N_{TEC} = 6$

The simulation model mimics the CAD design in figure 18. So it includes six IGBTs and six diodes as heat sources, a heat transfer coefficient h on the backside of the bottom DCB and six heat flux exit areas on top of the six TEC components. Three different operating modes of the converter module are simulated: Normal operation, an overload scenario with no increase of max junction temperature of IGBT and an overload scenario with $\Delta T_J = 5$ K permitted junction temperature rise.

As motivated earlier (section 2, figure 5), the given specifications of table 1 require $N_{TEC} = 12$, not 6. Under these boundary conditions, the total power per TEC $P_{TEC} = 4.7$ W. Therefore a reduced set of loading conditions is foreseen as given in table 8. Thermal boundary conditions are given in figure 19, using the reduced loading conditions given in table 8, the resulting temperatures in figure 21.

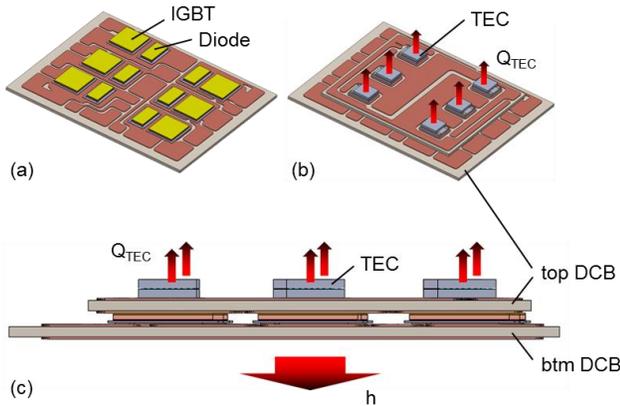


Fig. 19: Overview of model and thermal boundary conditions: Sixpack on bottom DCB (a), six TECs on top DCB (b), boundary conditions for FE model (c) as given in table 8, and total heat flux per TEC into buffer $P_{TEC} = 4.7$ W.

Solving the model led to a slightly asymmetrical temperature distribution in bottom DCB (see figure 20, left). IGBTs near the border are about $\Delta T_{geom} = 5$ K hotter. The reason for this is the slightly asymmetrical design of the entire module (see figure 19 bottom).

Table 8: Reduced overload conditions for $N_{TEC} = 6$

Operation	Normal ($T_J=125$ °C)	Overload +0K ($T_J=125$ °C)	Overload +5K ($T_J=130$ °C)
P_{IGBT} [W]	$10.1 \times 6 =$ 60.6	$13,87 \times 6 =$ 83.2	$14,82 \times 6 =$ 88.9
P_{Diode} [W]	$1.7 \times 6 =$ 10.2	$2.2 \times 6 =$ 13.2	$2.36 \times 6 =$ 14.2
$P_{OL,tot}$ [W] (red.)	0	25,6 (-40% to spec.)	32.3 (-25% to spec.)
P_{TEC} [W]	0	$4.7 \times 6 =$ 28.2	$4.7 \times 6 =$ 28.2
$P_{Backside}$ [W]	70.8	68.2	74.8
h [W/m ² /K]	1805 @ 70 °C		

By adjusting the models overload conditions one can determine for the given max. $P_{TEC} = 4.7$ W each for

$\Delta T_{j,max} = 0$ K and 5 K temperature rise the maximum allowed overload for IGBT and diode. By reducing $P_{OL,tot} = 43$ W to 25.6 W ($\approx -40\%$) for 0 K case or 32.3 W ($\approx -25\%$) for the 5 K case, the $\Delta T_{j,max}$ limit can always be met.

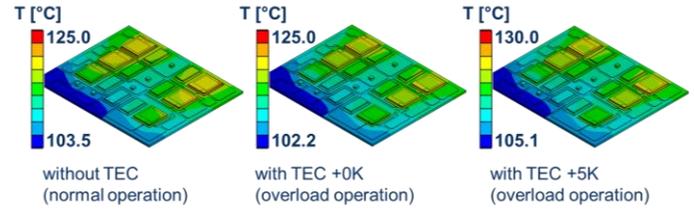


Fig. 20: Temperature field during normal operation (left) and overload operation with activated TE cooling (mid/right).

As result it can be stated that transient double sided cooling supported by TE cooling is suited to overcome transient overload situations in a power package. For more power to be pumped more efficient TECs would be, of course, desirable.

9. Joining Technologies Overview

Different assembly technologies can be applied for building double-sided cooling. They all rely on the achievement of hi-temperature interconnections.

Transient liquid phase bonding (TLPB) is one of the eligible technologies. Unlike established soldering used for first level die bonding of vertical power components like IGBTs and diodes, the solder material cannot remelt when operation temperature exceeds the soldering temperature. Effectively during joining, the thin solder layer melts and fully transforms into intermetallic compounds, shifting the temperature of liquid phase formation towards higher values. Due to the thinness of the solder layer, the reaction is completed within a very short time. After bonding the bondline consists in thermally stable phases, and no remelting of the joining material can occur. The bondline is to be kept at low bondline thicknesses also due to thermal considerations.



Fig. 21: Cross-section of a TLPS interconnect. Note the Cu particles surrounded by intermetallics.

A second alternative is sintering of silver powders. Powder is mixed with organics to form a paste which is afterwards applied by stencil printing onto the substrate. Variations in processing are considered, e.g. with or without pressure application during sintering, to obtain good bonding of the die with the substrate. During heating up, firing of the silver paste occurs, organics evaporate followed by densification of silver particles. Sintering occurs by atomic diffusion engendering a bulk silver bond with low or no porosity. As a consequence,

the resulting bondline has good heat transfer properties due to the very high conductivity [24] of the bond material and is thermally stable. Moreover, silver sintered interconnects depict higher reliability in thermal cycling tests than conventional SAC solders.

Transient liquid phase soldering (TLPS) represents the third alternative. Contrary to sinter silver sintering, the transient liquid phase soldering (TLPS) is a fully new developed joining technology based on a leadfree composition. Similar to TLPB, this solder based interconnection technology relies on phase transformation. Contrary to TLPB, which necessitates electroplating of the solder, TLPS is based on powder technology. Low and high melting powders are mixed together, typically Sn-based and copper powders. The resulting paste is applied by stencil printing and under the influence of temperature, the whole interconnect joint is transformed into intermetallics [25].

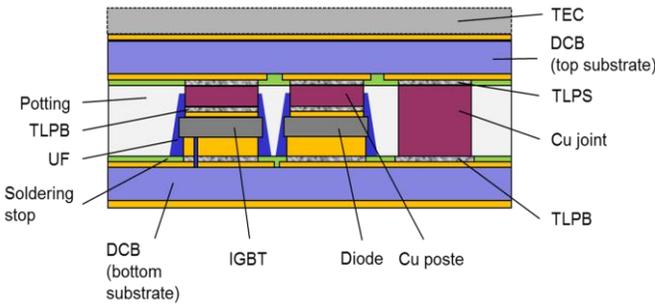


Fig. 22: *Joining technologies used to enable a process hierarchy. Note also the copper inserts to achieve required vertical spacing to assure high voltage insulation (postes) or electrical connection between top and bottom DCB (joint).*

A TLPS layer is thicker than a TLPB bondline since the process is based on powder (see figure 21). Intermetallics depict lower thermal conductivities than silver by approximately one order of magnitude (see table 6), potentially resulting in a higher thermal resistance of the joint. This has to be accounted for by thermal design.

10. Power module Assembly & Process Flow

The combination of the described technologies requires wafer level back end processes. First, active wafers must be post processed to obtain adequate surface finishes. Wafer post-processing includes temporary wafer bonding for safer handling and electroplating of copper and tin on the electrical contacts.

After dicing, diodes and IGBTs (voltage class 1200 V) are mounted per flip-chip on the DCB substrate. The gate and Emitter of the IGBTs and the anode of the diodes are connected face down to the substrate. The achieved TLPB bondline consists in a Cu_6Sn_5 intermetallic layer between two Cu_3Sn intermetallics layers formed by interdiffusion of copper and tin. The bondline thickness is in the range of some micrometers providing excellent thermal performance. Subsequently, an underfilling (UF) process is done to protect and insulate the connections. To build the inverter module, top-bottom electrical feedthroughs are required. Copper elements are added and also joined using the TLPB process.

Afterwards, the top DCB substrate is mounted on the backside of the components using one of the two others technologies previously described, ie. TLPS or silver sintering. This is schematically depicted in figure 22.

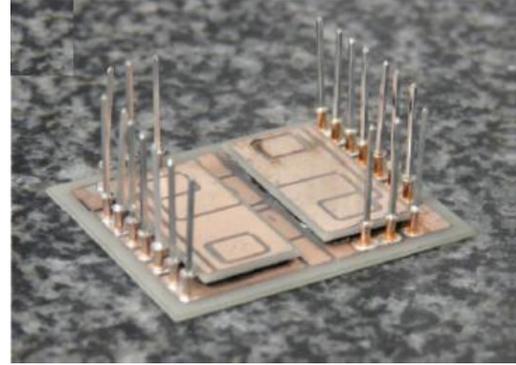


Fig. 23: *Double-sided cooling power module (double half bridge inverter module) after assembly, for testing purposes. It includes TLPB and TLPS as joining technology.*

One of the first fully mounted half bridge modules is shown in figure 24. Here TLPS has been used to contact the devices with the top DCB substrates. As can also be seen in figure 23, TECs can further be mounted on the top layer of the top DCB, where corresponding pads are foreseen for soldering.

12. Conclusions & Outlook

In this paper we have presented a system approach to a new thermal management concept for power devices featuring thermal buffering of transient overload scenarios controlled by thermo-electric devices in a situation where other solutions are not applicable.

In sum, we were able to show, using material characterisation, process development, experiment and simulation, these main results:

- The envisaged concept is able to thermally manage the thermal transients as required by industry for this specific application.
- Transient coupled-field simulations are used to predict thermal performance and are verified to very good agreement using various thermographic methods.
- An optimised configuration of the TECs and inner thermal buffer architecture for compact integration into the easyPIM casing could be devised and is being tested. The use of heat pipes was shown to be mandatory to bypass the low diffusivity limits of the phase change material, for which eutectic BiSn was found to be ideal.
- Newly developed die attach technologies like transient liquid phase soldering and bonding using the CuSn system and sintered silver allow a high-temperature capable, very low thermal resistance bond and enable a hierarchic process sequence as required to assemble a double-sided cooling module.

Next steps will include a system level experimental proof of concept w.r.t. thermal performance and thermo-mechanical aspects during stress testing.

Although the given example was motivated from requirements belonging to a niche application in industry, we are convinced that this approach will open up new degrees of freedom for the design of future power modules due to novel joining technology and thermal buffering and spin off to high-temperature electronics.

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